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High-frequency pulse width modulation implementation using FPGA and CPLD ICs

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Abstract

Pulse width modulation (PWM) has been widely used in power converter control. Most high power level converters operate at switching frequencies up to 500 kHz, while operating frequencies in excess of 1 MHz at high power levels can be achieved using the planar transformer technology. The contribution of this paper is the development of a high-frequency PWM generator architecture for power converter control using FPGA and CPLD ICs. The resulting PWM frequency depends on the target FPGA or CPLD device speed grade and the duty cycle resolution requirements. The post-layout timing simulation results are presented, showing that PWM frequencies up to 3.985 MHz can be produced with a duty cycle resolution of 1.56%. Additionally, experimental results are also presented for low cost functional verification of the proposed architecture.

Keywords: Pulse width modulation; Power converters; Field programmable gate array; CPLD; Counter

1. Introduction

The pulse width modulation (PWM) principle is widely used in power electronics applications for controlling power converters (DC/DC, DC/AC, etc.) [1]. The application of PWM control in a Buck-type DC/DC converter is shown in Fig. 1. The PWM control signal, V_{PWM} in Fig. 1(a), is used to control the power switch S and modulate the DC input voltage into a high-frequency wave, V_{oi}, which then passes through a lowpass L-C filter producing the DC output voltage, V_o. The PWM signal is generated by comparing an adjustable reference voltage, V_{ref}, with a triangular wave of constant amplitude and frequency, as shown in Fig. 1(b). The DC output voltage is regulated to the desired value by adjusting the reference voltage value, thus modifying the PWM signal duty cycle, as follows:

$$V_o = D \cdot V_{in} = \frac{t_{on}}{T_s} \cdot V_{in} = \frac{V_{ref}}{V_{tr}} \cdot V_{in} \quad (1)$$

where V_{in} is the converter DC input voltage, D is the PWM signal duty cycle ($0 \leqslant D \leqslant 1$), t_{on} is the PWM signal ON time, T_s is the converter switching period and V_{tr} is the triangular wave amplitude. The power switch is usually of MOSFET or IGBT type, while the power inductor is wound on a ferrite core. Ferrite cores are magnetic materials capable of

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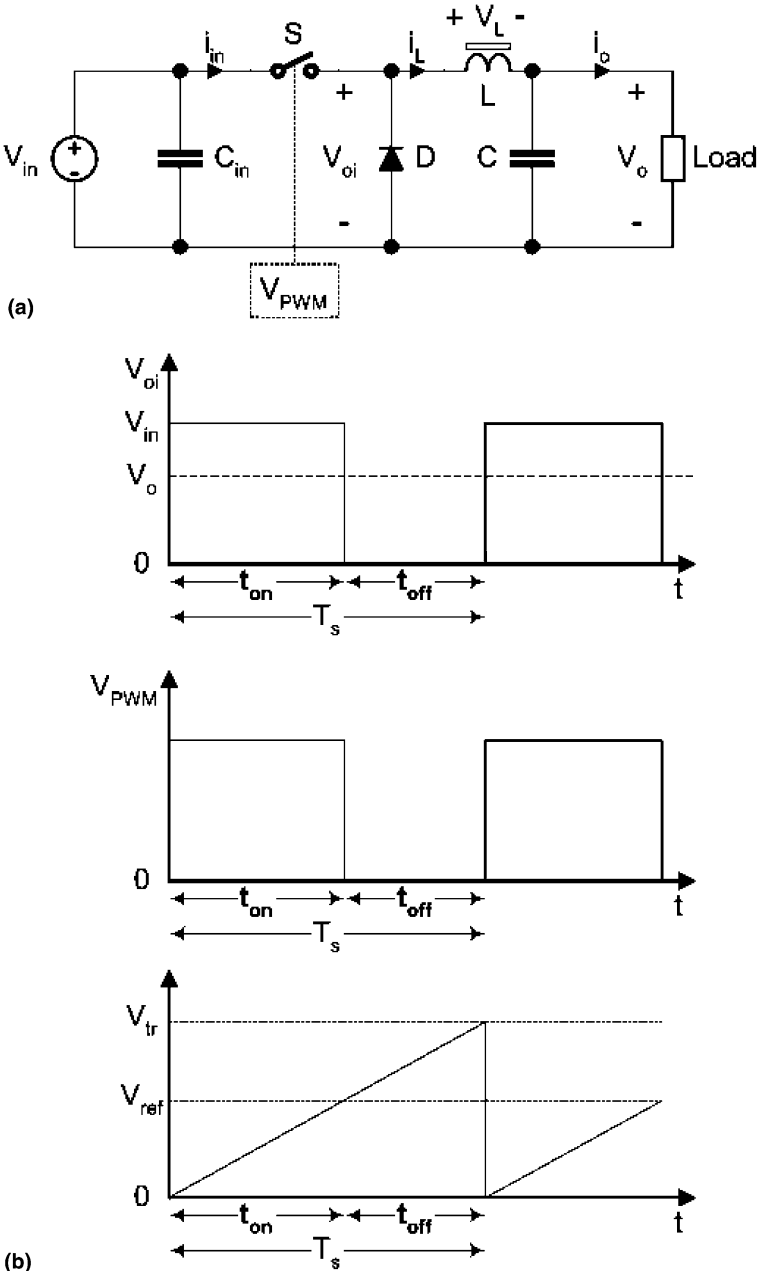

Fig. 1. PWM control of a buck-type DC/DC converter: (a) power converter diagram and (b) associated waveforms.

operating at frequencies up to several hundreds of kHz with low losses, while their size is inversely proportional to the operating frequency. Since the power converter size and weight mainly depend on the magnetic material geometry, it is essential to increase the switching frequency in order to reduce the converter size. Currently, most power converters operate at frequencies up to 500 kHz [2,3] due to limitations of power semiconductor and magnetic material technology at both, high frequency and power levels. However, converter operating frequencies in excess of 1 MHz at high power and efficiency levels can be achieved using the planar transformer technology [4].

The PWM control strategy has also been applied in zero voltage and zero current switching (ZVS and ZCS, respectively) resonant converters [5], which have the advantages of lower electromagnetic

emission and higher operating frequency capability, compared to the hard-switching converter implementation described above. In all design methods, the switching frequency selection is a compromise between the power switch losses and the magnetic components power losses.

In many applications it is desirable to control a power converter using a microcontroller or a digital signal processor (DSP) for the implementation of sophisticated control schemes such as fuzzy control [6], renewable energy sources control [7], etc. The block diagram of such a configuration is depicted in Fig. 2(a). A set of sensors, used to measure the power converter signals of interest, such as the output current or voltage, output frequency, etc., are interfaced through an Analog to Digital (A/D) converter to a microcontroller or DSP unit. The measured parameters are input to a digital controller in order to adjust the duty cycle value of the PWM signals, which further control the power converter operation, according to the desired control law, such as fuzzy logic control, PID control, neural networks control, etc. Since it is desirable to integrate all operations in a single IC for reduction of the total system cost, each PWM signal is usually generated using an on-chip PWM generator, built according to the general block diagram shown in Fig. 2(b). An N-bit value, corresponding to the desired duty cycle value, is compared with the value of an N-bit counter running with clock frequency f_{clock}. The comparator output is used to trigger a toggle register, producing a PWM output signal with adjustable duty cycle value. This configuration has the disadvantage that the resulting signal frequency, which defines the power converter switching frequency, is limited by the microcontroller or DSP unit clock frequency. Using an N-bit resolution, resulting in 2^N different duty cycle states, the clock frequency, f_{clock}, is related to the PWM output wave frequency, f_{PWM}, as follows:

$$f_{\text{PWM}} = \frac{f_{\text{clock}}}{2^N} \tag{2}$$

Assuming that an 8-bit resolution is desired, then the required clock speed for a 100 kHz PWM signal is 25.6 MHz, while for a 500 kHz PWM frequency output the required clock frequency is 128 MHz, which cannot be supported by a microcontroller

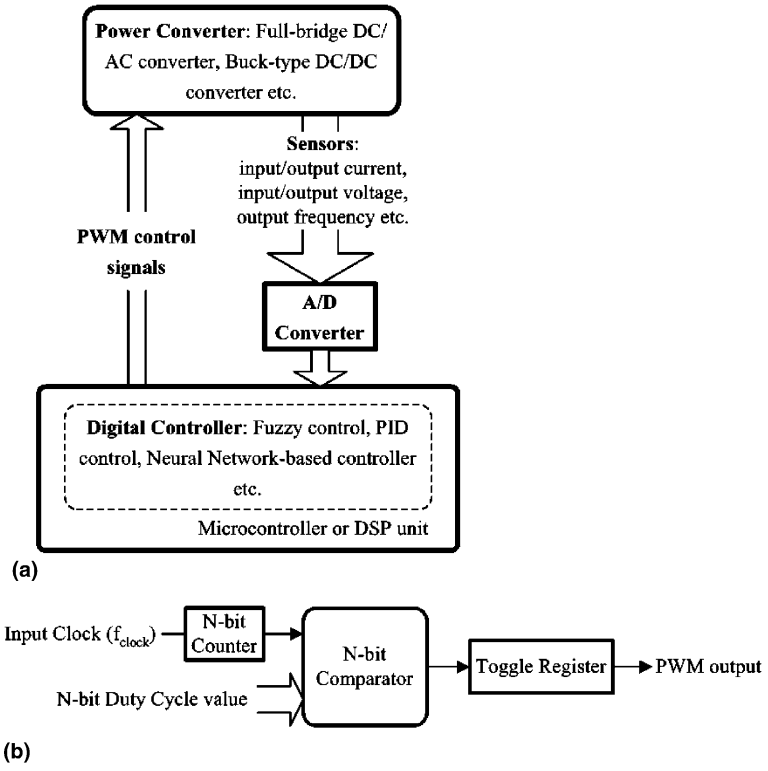

Fig. 2. Implementation of digital power converter control using a microcontroller or DSP unit: (a) the general block diagram and (b) the PWM generator architecture.

or DSP unit. If the PWM generator is implemented in software, then a number of instructions is required, each one executed in state times which are multiples of the microcontroller clock period, also resulting in a low PWM frequency and/or resolution. In an alternative version, a Digital to Analog (D/A) converter is used to convert a digital word to the corresponding analog reference voltage, which is then compared with a triangular wave in order to produce the PWM signal [8]. This method has the following disadvantages: (a) the PWM generation unit is sensitive to noise and component value variations and (b) the system cost is increased because additional components are required.

The PWM generation techniques, which have been used to develop digital controllers for low power switching power supplies are shown in Fig. 3(a) and (b) [9,10]. The architecture shown in Fig. 3(a) is based on the same principle with the configuration presented in Fig. 2(b). A counter is triggered by a clock signal, f_{clk}, with frequency equal to some multiple of the power converter switching frequency, f_{sw}. The PWM output signal is set to logical "1" at the beginning of the switching period and is reset after a number of clock cycles equal to the integer value of the N-bit data input. The disadvantage of this method is that a high clock frequency is required, resulting in increased power dissipation. In the delay-line-based PWM circuit, shown in Fig. 3(b), a pulse from a reference clock starts a cycle and after a certain delay, designed to match the propagation delay experienced through the multiplexer, sets the PWM output to high. The reference pulse propagates through the delay line and when it reaches the output selected by the multiplexer its value is used to set the PWM output to low. The total delay through the delay line is calculated to be equal to the reference clock period. The drawback of this method is that the implementation area requirements grow exponentially with the multiplexer resolution bits N. Aiming towards a compromise between area and power requirements, a hybrid delay-line/counter approach [11] is presented in Fig. 3(c). An N-bit PWM resolution is achieved

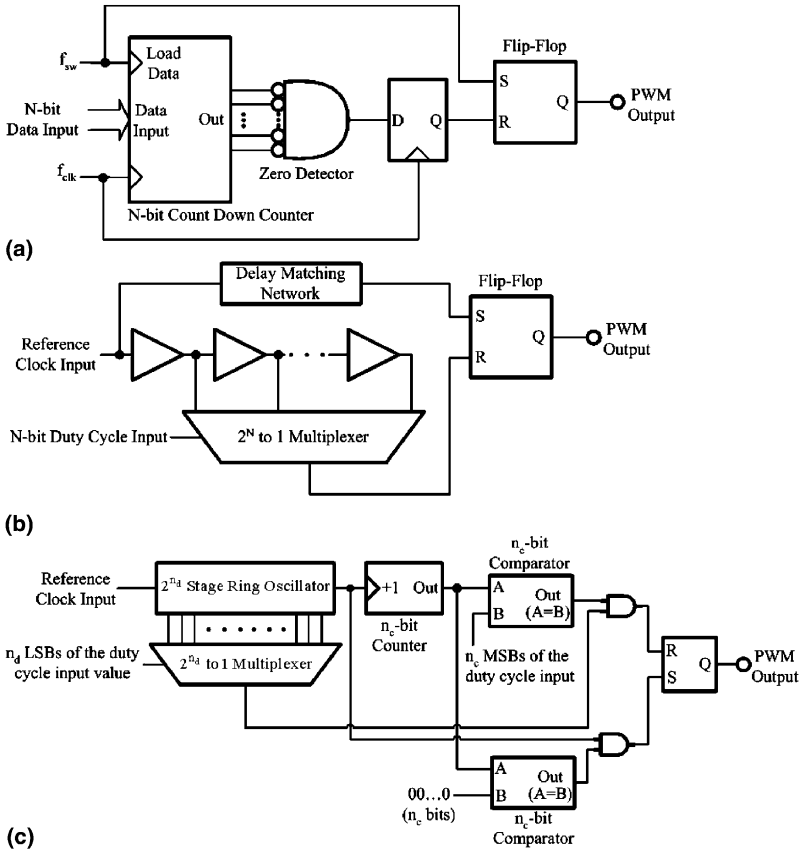

Fig. 3. PWM generator topologies: (a) the counter-based, (b) the delay-line and (c) hybrid delay-line/counter architectures.

using an n_c-bit counter and an n_d-bit delay-line, designed such that $N = n_c + n_d$. The delay-line has been built with D-type flip-flops comprising a ring oscillator. The PWM output frequency, in this case, is given by the following equation:

$$f_{PWM} = \frac{f_{clock}}{2^{n_c}} \quad (3)$$

Using this configuration, the digital controller presented in [11] achieves a 1 MHz PWM frequency with an 8-bit resolution using a 3-bit counter and a 32-cell long ring oscillator. The required clock frequency is 8 MHz, while a PWM generator built according to the counter-based approach would require the substantially higher clock frequency of 256 MHz for equal duty cycle resolution. However, both the 32-cell ring oscillator and the 32:1 multiplexer result in large implementation area requirements. The delay-line and the hybrid counter/delay line architectures have been primarily developed for the design of digital circuits used to control low output voltage (<2.7 V) and low output power (<3 W) converters, where the control circuit power consumption must be minimized, since it highly affects the overall power conversion efficiency.

The development of field programmable gate array (FPGA) and complex programmable logic device (CPLD) ICs during the last years provides an alternative solution for the implementation of digital power converter control units. They have the advantage of flexibility due to their reprogramming capability, while their operating frequency can be as much as hundreds of MHz. FPGAs have been used in power electronics applications for the implementation of complicated control schemes, such as fuzzy logic control of a DC/DC converter [12] and deadbeat control of a three-phase DC/AC inverter [13]. The power converters FPGA-based digital control units presented in [14–17] include PWM generator modules built according to the counter-based design principle described above. The PWM signals produced feature frequencies which range from 9 kHz up to 31.25 kHz, but their operation at higher frequencies has not been investigated. In [18] a Xilinx SPARTAN II FPGA IC is used for the development of a PWM generator unit. The resulting PWM frequency range is 1 kHz up to 200 kHz with a duty cycle resolution of 1% and in addition PWM waveforms of 13.33 kHz were presented in the experimental results.

In this paper, a novel architecture for the implementation of high-frequency PWM generation units for power converter control using FPGA and CPLD ICs is presented. The implementation of FPGA-based digital control schemes is economically feasible when applied to power converters of moderate power level (e.g. over 100 W) so the proposed system is designed according to the counter-based architecture described above. Although it is operating at a higher clock frequency resulting in higher power dissipation, as compared to the delay-line and hybrid delay-line/counter design methods, this power dissipation is negligible taking into account the target converter power capability. Additionally, the counter-based architecture has the advantage of lower area consumption, which is critical in case that complex control schemes with large area requirements are to be implemented in the same FPGA or CPLD IC. The proposed PWM generation unit is based on a specially designed, synchronous binary counter, resulting in maximum PWM frequencies up to 3.985 MHz with a duty cycle resolution of 1.56%, while the PWM unit can be easily interfaced to a microcontroller or DSP system. The resulting PWM frequency depends on the target FPGA or CPLD device speed grade and the duty cycle resolution required. The high-frequency performance of the proposed digital PWM generator unit is demonstrated using post-layout timing results, which are considered to be rather conservative compared to practical conditions, while, additionally, experimental results are presented for frequencies up to 781.25 kHz for low cost functional verification of the proposed architecture.

The proposed PWM architecture is described in Section 2, while the simulation and experimental results are presented in Sections 3 and 4, respectively.

2. The proposed PWM architecture

The block diagram of the proposed architecture is shown in Fig. 4. The system input is an N-bit data word, corresponding to the desired PWM duty cycle value, so that it can be easily interfaced to a microcontroller unit I/O port pins. The N-bit register output, containing the N-bit data input, is compared with the output value of an N-bit free-running synchronous counter, by means of a comparator. When these two values become equal, the comparator output is used to reset the R/S latch output which produces the PWM wave. The R/S latch output is set when the counter reaches an overflow condition at

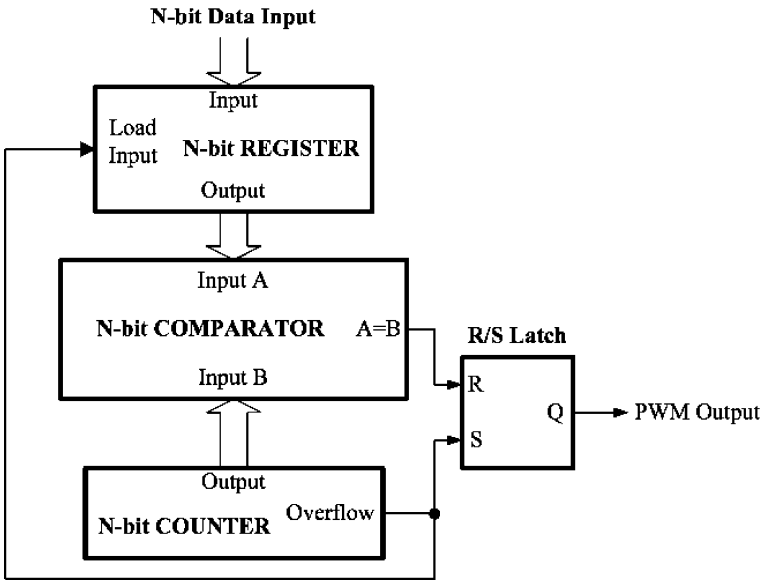

Fig. 4. Block diagram of the proposed PWM generator.

the end of a PWM period. Also, the counter overflow signal is used to load the N-bit data input to the input register, so that the PWM output duty cycle change is performed at the new PWM wave period in order to avoid any frequency and/or phase jitter of the output waveform. The PWM frequency is given by Eq. (2), while its duty cycle is given from the following equation:

$$D = \frac{\text{Data\_Value}}{2^N} \tag{4}$$

where Data_Value is the input data word integer value.

If an 8-bit input is used, then the duty cycle is in the range $0 \leqslant D \leqslant \frac{255}{256} = 99.6\%$. Since the PWM duty cycle has 2^N different states, the generator resolution, α, is defined as

$$\alpha = \frac{1}{2^N} \cdot 100\% \tag{5}$$

In order to achieve high PWM frequencies, resulting in high clock rates, a fast counter is required. Synchronous counters have the inherent characteristic that the latency related to the state decoding bounds the maximum permissible clock frequency, thus an alternative design method has to be introduced. The block diagram of the fully synchronous free-running counter implemented is shown in Fig. 5 and the corresponding timing diagram presenting the associated waveforms is depicted in Fig. 6. The counter has been built around: (a) toggle flip-flops, $T_0 \ldots T_{N-1}$, corresponding to the counter output bits $C(0) \ldots C(N-1)$ and (b) a combination of D-type flip-flops, $D_1 \ldots D_{N-1}$, with outputs $Q(1) \ldots Q(N-2)$ and AND gates, $G_1 \ldots G_{N-1}$, comprising the state decode logic within the counter. All flip-flops are clocked with a common clock signal, f_{clock} and if a toggle flip-flop input, EN, is set, then its output, T, is toggled at the next clock pulse. The reduction of the time associated with the counter state decoding is critical, in order to enhance the counter high-frequency operation capability and is based on predicting each counter output state change, before the actual time that this change must be accomplished. Thus, each D-type flip-flop, D_i, is used to prepare the subsequent toggle flip-flop, T_{i+1}, output state change, by setting the corresponding input one cycle before this change must take place. Also, each AND gate, G_i, is used to predict the $C(i+1)$ counter output state change two clock cycles before the clock cycle that this change must be executed. Finally, the counter "Overflow" signal is produced by the D_{N-1} flip-flop at the end of the PWM period and is used to load the new duty cycle value to the PWM generator input register.

In order to produce the clock input, the PLL-based Cypress CY2308 zero delay buffer, the Motorola MC88915 and MPC9331 clock generators and the MPC9229 clock synthesizer can be used to multiply a reference frequency up to 400 MHz. The reference frequency can be supplied from 12 to 25 MHz crystal or any other clock source available,

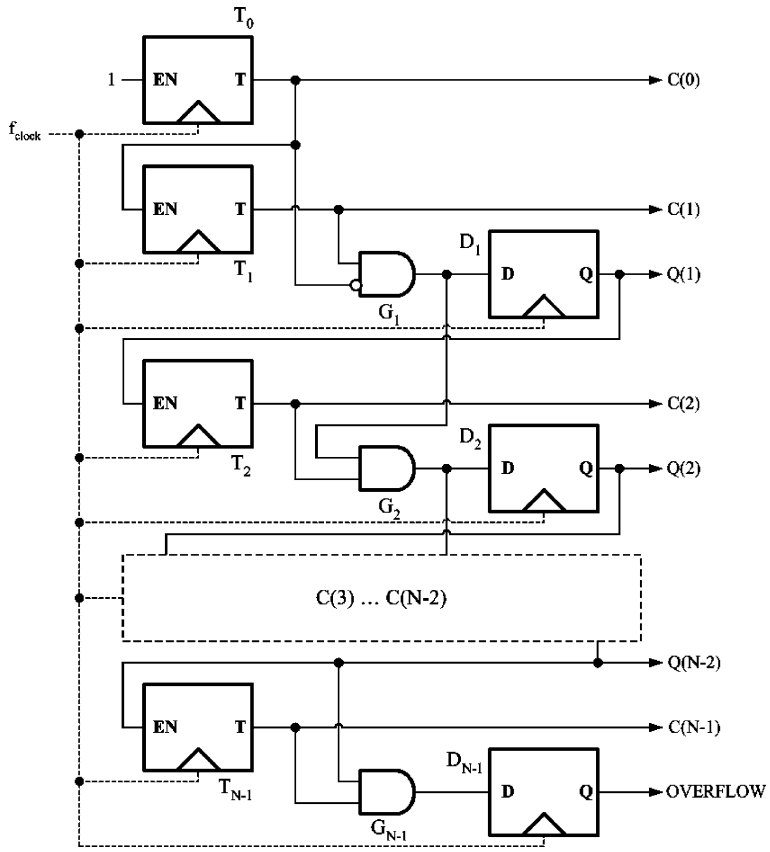

Fig. 5. Block diagram of the counter.

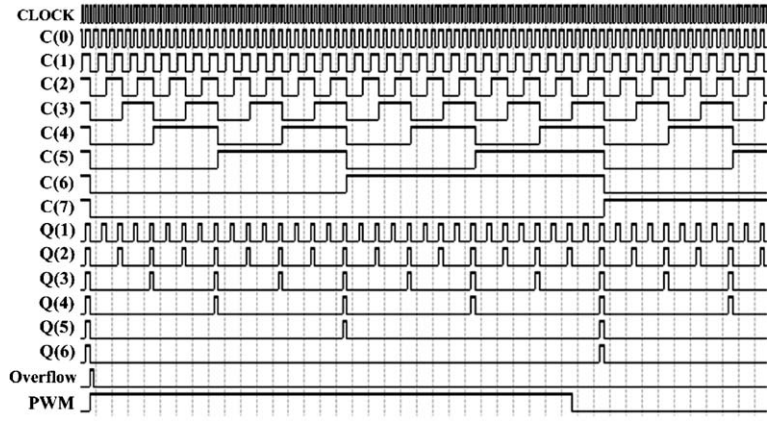

Fig. 6. Timing waveforms of the counter.

while the ICs can be arranged in tree configurations to meet the design clock requirements. If a Xilinx VIRTEX or SPARTAN-II FPGA is used, then the on-chip delay-locked-loops can be used to multiply the input clock and eliminate any clock delay within the device.

3. Simulation results

A software program using the VHDL language was developed, for synthesizing the architecture presented in the previous section, using the Xilinx Foundation software v3.1. The Foundation Soft-

ware timing analyzer is used for various devices manufactured by Xilinx, such as the FPGAs XC4000XLA, XC4000XL, SPARTAN-II and VIRTEX, as well as the XC9500 CPLD families. The resulting post-layout maximum clock frequencies, achieved by the proposed system for 8-bit data input configuration of the PWM generation unit, are shown in Tables 1–3, respectively. The corresponding maximum PWM signal frequency, the device cost and the FPGA Configurable Logic Blocks (CLB) used are also presented. It can be observed that the implementation of the proposed architecture occupies only a small percentage of the corresponding device logic blocks, thus permitting the integration of additional control operations in the same IC. Also, the timing simulation results have shown that the maximum clock speed is mainly bounded by the architecture logic delays being about 65% of the clock period, compared to about 35% of routing delays.

The maximum clock frequency and the maximum PWM signal frequency for 8, 7 and 6-bit data input configurations, are tabulated in Table 4. The resulting PWM resolutions are 0.39%, 0.78% and

Table 1
Post-layout timing results for the Xilinx XC4000XLA and XC4000XL families

Device type	Max. clock frequency (MHz)	PWM frequency (MHz)	Cost ($)	CLBs used
XC4013XLA-07PQ160	184.877	0.722	111.1	19 out of 576
XC4020XLA-07PQ160	174.155	0.680	140.8	19 out of 784
XC4028XLA-07HQ160	178.540	0.697	240.9	19 out of 1024
XC4010XL-3PC84	94.127	0.367	48.6	19 out of 400
XC4005XL-09PC84	145.096	0.566	73.2	19 out of 196

Table 2
Post-layout timing results for the Xilinx SPARTAN-II and VIRTEX families

Device type	Max. clock frequency (MHz)	PWM frequency (MHz)	Cost ($)	Slices used
XC2S100-6TQ144	205.044	0.8	22.3	17 out of 1200
XC2S15-6TQ144	200.240	0.782	10.3	17 out of 192
XC2S150-6PQ208	209.952	0.820	27.3	17 out of 1728
XCV100-6TQ144	202.224	0.789	167.2	17 out of 1200
XCV100-6PQ240	198.570	0.775	191.4	17 out of 1200
XCV50-6PQ240	206.186	0.805	102.4	17 out of 768

Table 3
Post-layout timing results for the Xilinx XC9500 CPLD family

CPLD type	Max. clock frequency (MHz)	PWM frequency (MHz)	Cost ($)	Macrocells used
XC9536-5PC44	90.9	0.355	10.8	28 out of 36
XC9572-10PC44	62.5	0.244	8.4	25 out of 72
XC95144-10TQ100	62.5	0.244	31.6	25 out of 144

Table 4
Post-layout timing results for various PWM resolutions

Device type	8-bit Resolution		7-bit Resolution		6-bit Resolution	
	Maximum clock frequency (MHz)	Maximum PWM frequency (MHz)	Maximum clock frequency (MHz)	Maximum PWM frequency (MHz)	Maximum clock frequency (MHz)	Maximum PWM frequency (MHz)
XC2S100-6TQ144	205.044	0.8	226.706	1.771	244.978	3.827
XCV100-6TQ144	202.224	0.79	233.318	1.822	239.981	3.749
XC4013XLA-07PQ160	184.877	0.722	203.666	1.59	255.102	3.985
XC4010XL-3PC84	94.127	0.367	127.665	0.997	135.355	2.11
XC9536-5PC44	90.9	0.355	100.0	0.781	100.0	1.56

1.56%, respectively. The maximum clock speed is increased if the PWM resolution is reduced, because of the delay reduction associated with the counter internal logic.

Observation of the results presented above, reveals that PWM frequencies up to 3.985 MHz can be produced using the proposed design method with a duty cycle resolution of 1.56%, which is adequate for a number of applications such as motor control, renewable energy systems control, etc. A plot of the resulting maximum PWM frequency versus the FPGA or CPLD device type for duty cycle

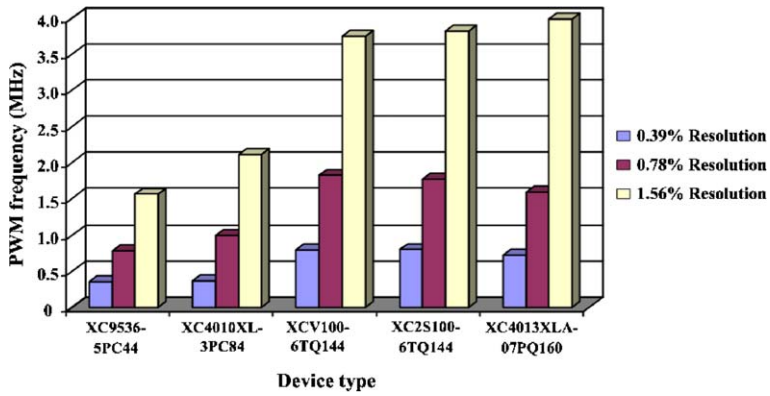

Fig. 7. The post-layout resulting maximum PWM frequency versus the FPGA or CPLD device type for various duty cycle resolution values.

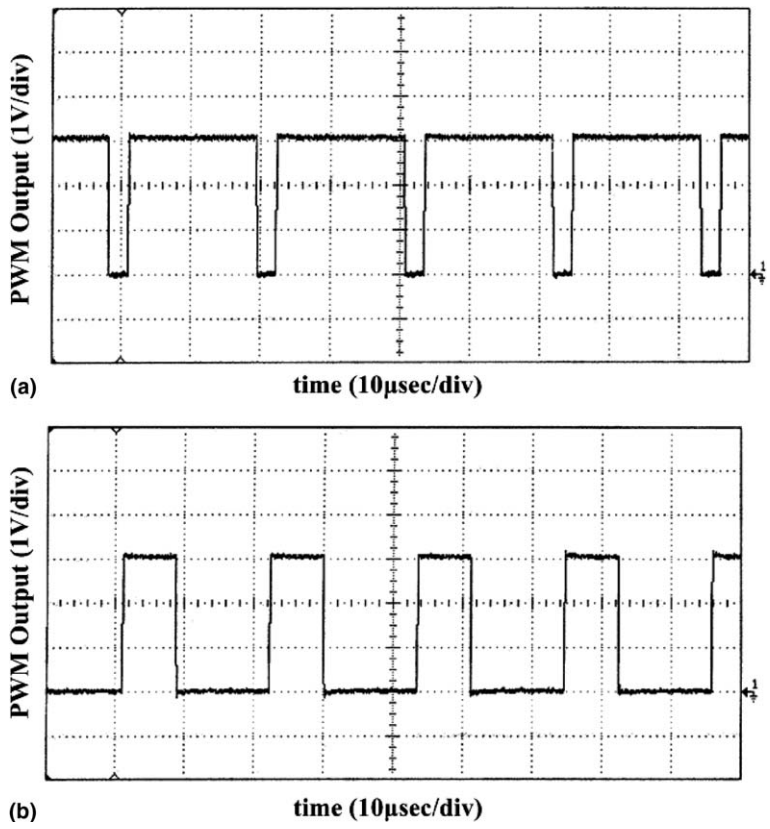

Fig. 8. Oscilloscope waveforms of the PWM output for various duty cycle values: (a) 86.71% and (b) 36.71%.

resolution values of 0.39%, 0.78% and 1.56%, respectively, is presented in Fig. 7. A lower duty cycle resolution value corresponds to better resolution step. It is observed that the PWM frequency depends on the target device speed grade and the duty cycle resolution. The FPGA or CPLD device type is selected according to the digital control system implementation area and cost requirements. In case that the desired PWM frequency can be achieved with high (worse) duty cycle resolution for the selected FPGA or CPLD IC, then duty cycle dithering techniques can be easily combined with the proposed methodology in order to enhance the resolution of the resulting duty cycle values [19].

The timing analyzer is rather conservative and the maximum clock frequency that can be achieved using the proposed system, under practical conditions, can be considerably higher compared to the simulation results. Thus, the post-layout timing results are frequently used to analyze and demonstrate the performance of FPGA designs [20]. Furthermore, the maximum clock frequency can be further increased using manual placement techniques, during the device configuration stage [21].

4. Experimental results

The proposed architecture operation was verified using the XS40 v1.2 board, which contains the Xilinx 4010XLPC84-3 FPGA and the post-layout timing results of the implementation for this device are shown in Tables 1 and 4. The on-board clock running at 12 MHz was used and the resulting PWM frequency with an 8-bit data input was 46.875 kHz. The oscilloscope waveforms of the PWM output for 86.71% and 36.71% duty cycle values are shown in Fig. 8(a) and (b), respectively. The output waveform for a 7-bit data input implementation, resulting in a 93.75 kHz PWM frequency, is shown in Fig. 9(a). The PWM duty cycle is externally adjusted to 24.25%. The corresponding output waveform for a 6-bit data input implementation is shown in Fig. 9(b). The resulting PWM frequency in this case is 187.5 kHz, while the duty cycle is adjusted to 40.6%.

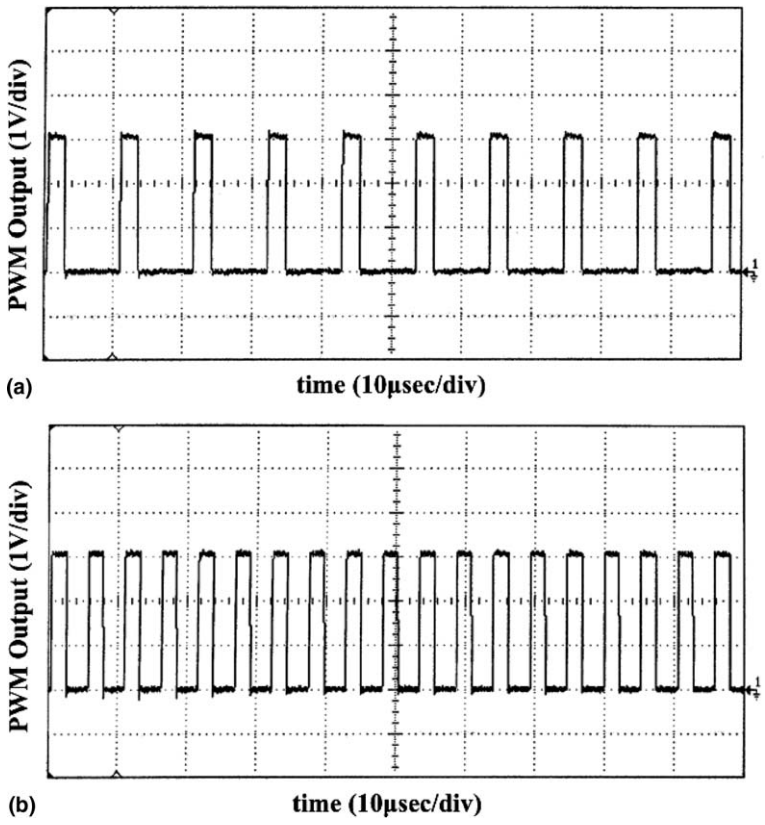

Fig. 9. Oscilloscope waveforms of the PWM output for two different data input length implementations: (a) 7-bit input and (b) 6-bit input.

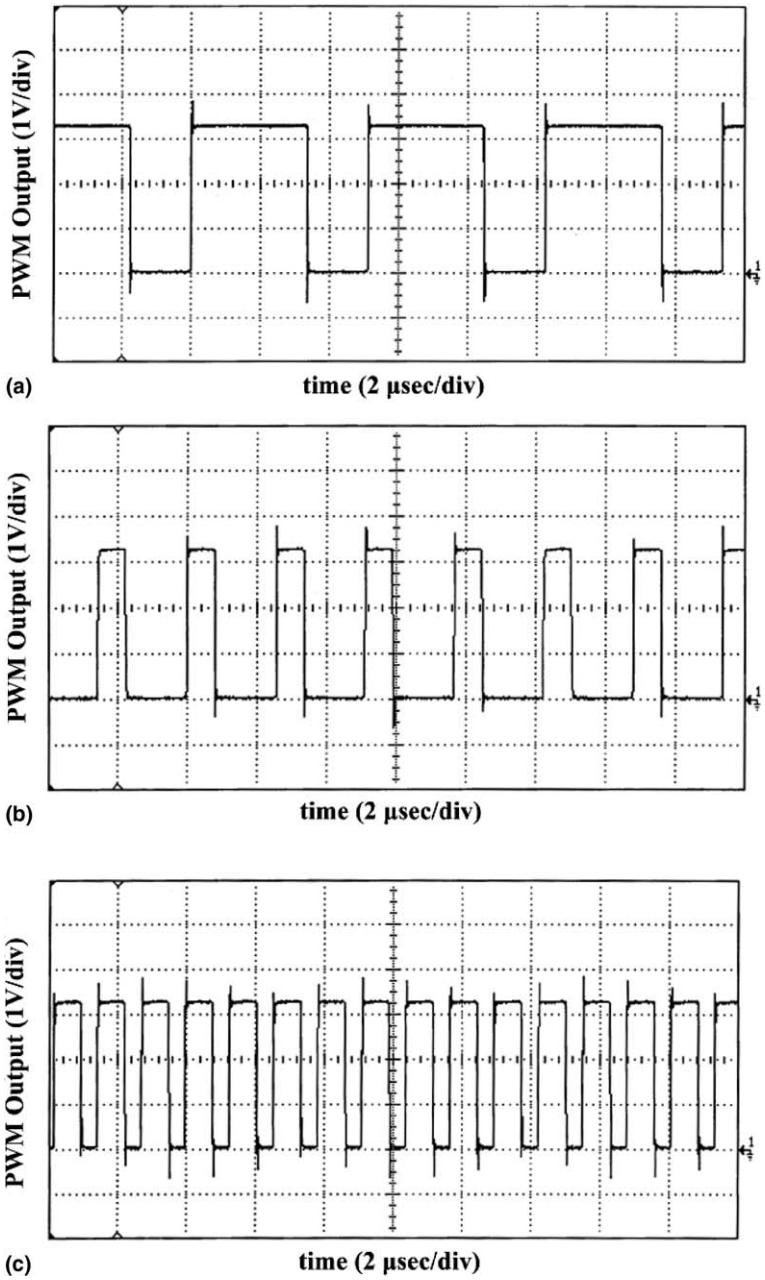

Fig. 10. Oscilloscope waveforms of the PWM output for three different data input length implementations using the Altera ACEX1K series EP1K10TC100-3 FPGA and a 50 MHz clock input: (a) 8-bit input (b) 7-bit input and (c) 6-bit input.

The high-frequency operation of the proposed PWM generator was also laboratory investigated using the Morph-IC development board (manufactured by Future Technology Devices International Ltd.) hosting the Altera ACEX1K series EP1K10TC100-3 FPGA and a 50 MHz oscillator, which has been used as the clock input of the PWM generator unit. The VHDL program modeling the proposed architecture has been synthesized using the QUARTUS II v4.2 software. According to the compilation report, the maximum clock frequency of the proposed system is 200 MHz for 8, 7, and 6-bit data input implementations, while the total logic elements required are 5%, 4% and 3%, respectively, out of the 576 logic elements contained in the EP1K10TC100-3 FPGA. The pro-

posed system has been tested for all combinations of data input values and the measured duty cycle values resulted equal to the theoretically expected ones. A subset of the above measurements is presented below. The oscilloscope PWM output waveform for an 8-bit data input implementation is shown in Fig. 10(a). The value of the data input has been externally set to 10101000 corresponding to a duty cycle of 65.62% while the measured PWM output frequency is 195.31 kHz. The output waveform for a 7-bit data input implementation, resulting in a 390.62 kHz PWM frequency, is shown in Fig. 10(b). The data input value has been set to 0101000 and the resulting duty cycle value is 31.25%. Finally, the PWM output waveform in case of a 6-bit data input implementation is shown in Fig. 10(c). The resulting PWM frequency is 781.25 kHz, while the duty cycle value has been set equal to 62.5% by applying the 101000 binary string to the PWM generator data input pins.

The PWM frequencies presented above are lower compared to the simulation results analyzed in Section 3, since low cost systems with low clock frequency generators were used only for functional verification of the proposed architecture. However, by selecting the appropriate FPGA or CPLD device type and the corresponding clock frequency generator, the proposed system performance at the higher clock frequency levels, presented in the previous section, can be achieved under any practical conditions, due to the high accuracy of the post-layout timing analysis results.

5. Conclusions

In this paper, a high-frequency PWM generator architecture for power converter control, using FPGA and CPLD ICs, has been presented. The proposed architecture is based on a special design synchronous binary counter and can be easily interfaced to a microcontroller or DSP system. The post-layout timing simulation results prove that using the proposed method, PWM frequencies up to 3.985 MHz can be produced with a duty cycle resolution of 1.56%, which is adequate for most applications. The resulting PWM frequency depends on the target FPGA or CPLD device speed grade and the duty cycle resolution required. The low percentage of the device logic blocks occupied by the PWM implementation permits the integration of multiple control operations in a single IC. The selection of the target device depends on the system cost and resolution requirements.

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