Development of an FPGA-Based SPWM Generator for High Switching Frequency DC/AC Inverters

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***Abstract*—The digital implementations of Sinusoidal Pulse Width Modulation (SPWM) generators have dominated over their counterparts based on analog circuits. In this paper, an FPGA-based SPWM generator is presented, which is capable to operate at switching frequencies up to 1 MHz (requiring FPGA operation at 100–160 MHz), thus it is capable to support the high switching frequency requirements of modern single-phase dc/ac power converters. The proposed design occupies a small fraction of a medium-sized FPGA and, thus, can be incorporated in larger designs. Additionally, it has a flexible architecture that can be tuned to a variety of single-phase dc/ac inverter applications. The postlayout simulation and experimental results confirm that compared to the past-proposed SPWM generation designs, the SPWM generator presented in this paper exhibits much faster switching frequency, lower power consumption, and higher accuracy of generating the desired SPWM waveform.**

***Index Terms*—DC/AC inverter, field programmable gate array (FPGA), high frequency, sinusoidal pulse width modulation (SPWM).**

I. Introduction

THE dc/ac converters (inverters) are the major power electronic conversion units in renewable energy production, motor drive, and uninterruptible power supply applications [1]–[4]. A simplified block diagram of a single-phase, full-bridge dc/ac power converter (inverter) is depicted in Fig. 1.

The Sinusoidal Pulse Width Modulation (SPWM) technique is widely employed in order to adjust the dc/ac inverter output voltage amplitude and frequency to the desired value. In this case, the power converter switches (e.g., MOSFETs, IGBTs, etc.) are set to the ON or OFF state according to the result of the comparison between a high-frequency, constant-amplitude triangular wave (carrier) with two low-frequency (e.g., 50 Hz) reference sine waves of adjustable amplitude and/or frequency [5], [6]. In the unipolar SPWM technique illustrated in Fig. 2, the generated pulses are either positive or negative during each half-period of the SPWM wave. The high-frequency harmonics of the generated SPWM signal, $V_{\rm spwm}$ in Fig. 2, are then filtered using

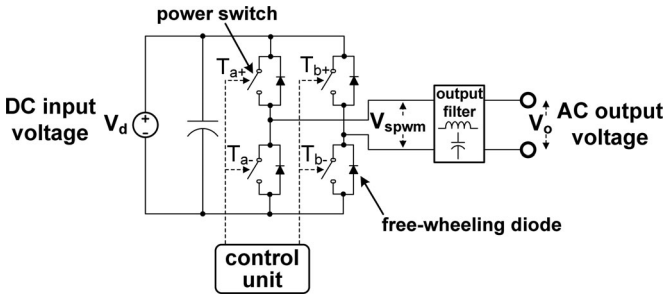

Fig. 1. Block diagram of a single-phase, full-bridge dc/ac power converter.

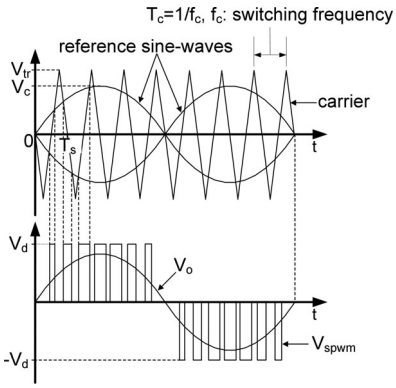

Fig. 2. Unipolar SPWM technique.

a low-pass *LC*-, *LCL*- or *LLCL* type filter [5], [7], thus producing the high-power and low-frequency sinusoidal waveform V_o at the output terminals of the dc/ac inverter. The amplitude of V_o (V) is calculated as follows:

$$\widehat{V_o} = M \cdot V_d = \frac{\widehat{V_c}}{\widehat{V_{\rm tr}}} \cdot V_d \tag{1}$$

where V_d (V) is the dc input voltage of the dc/ac inverter, $\widehat{V_c}$, $\widehat{V_{\rm tr}}$ (V) are the amplitudes of the reference sine and carrier signals, respectively, and M is the modulation index.

Increasing the switching frequency of the triangular wave f_c results in a reduction of the dc/ac inverter output filter size and cost [8]. Depending on their nominal power rating, the dc/ac inverters typically operate at switching frequencies in the range of 1–100 kHz [9], [10]. A dc/ac inverter comprised of four cascaded Z-source inverter modules, which have been built using Gallium Nitride devices operating at a 1-MHz switching frequency, is proposed in [11]. This trend of increasing the operating switching frequency is expected to continue in the near future [12], [13] due to the recent development of Silicon Carbide power semiconductors, such as JFETs, MOSFETs,

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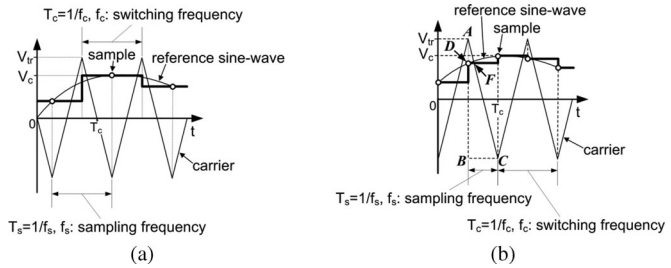


Fig. 3. Reference sine-wave digital representation in past-proposed SPWM generator design methods: (a) sampling at the nadirs and (b) sampling at both the nadirs and the peaks of the carrier wave.

and Schottky diodes [14]–[18], which are capable to operate at switching frequencies up to 3 MHz with low-power losses [19]. Thus, in case that this semiconductor technology is applied then a tenfold increase of the switching frequency is predicted in [20], compared with that of the conventional dc/ac inverters.

The digital SPWM generator implementations have dominated over their counterparts based on analog circuits, since they offer higher noise immunity and less susceptibility to voltage and temperature variations [21]. Typically, microcontrollers, Digital Signal Processors (DSPs) or Field Programmable Gate Arrays (FPGAs) are used for the implementation of the SPWM generation unit and the execution of dc/ac inverter control algorithms (e.g., output voltage regulation, fuzzy logic, motor speed control, etc.) [22]. The integration of both the control and SPWM subsystems in the same chip has the advantage of reducing the design complexity and the total system cost [23], [24]. However, the microcontroller- [25] and DSP-based [26], [27] implementations of the SPWM generator units developed so far operate at low switching frequency levels (i.e., 1–10 kHz). As discussed in [28], the computational speed of microprocessors and DSPs imposes an upper limit on the maximum switching frequency that can be generated using software-based SPWM generation techniques.

Using FPGAs for the development of the dc/ac inverter control logic has widely emerged during the last years since they are considered as a powerful and cost-effective solution [29]. Compared to the microcontroller and DSP-integrated circuits, FPGAs have the advantage of flexibility in case of changes and they enable the reduction of the execution time of the dc/ac inverter control algorithm due to their capability to integrate digital hardware with high speed and parallel processing features [30]–[35].

In the FPGA-based SPWM generation units presented in [21], [24], [36]–[41], the triangular wave is implemented in the form of an up-down counter. Depending on the implementation, the reference sine wave is sampled with a sampling frequency equal to f_s (regular-sampled pulse width modulation (PWM)) at the time instants corresponding either only to the nadirs [see Fig. 3(a)], or only to the peaks (symmetric modulation), or both at the nadirs and the peaks of the carrier wave [asymmetric modulation, Fig. 3(b)]. The corresponding samples are stored in digital format in a lookup table (LUT) implemented in the FPGA internal memory. The SPWM control signals are produced by comparing the corresponding values of the sinusoidal and carrier digital signals. Using these techniques, SPWM switching frequencies in the range of 1.157–20 kHz have been achieved. The same design method has been applied in [23] for the development of an SPWM signal generation SoC based on the OpenRISC1200 32-bit RISC processor core.

Targeting at the reduction of the SPWM generator memory requirements, the sinusoidal wave is produced in [42] using an FPGA-based implementation of the Coordinate Rotation Digital Computer (CORDIC) algorithm. A 5-kHz switching frequency has been achieved in this case. Although this implementation does not require the use of a hardware multiplier, it is characterized by a slower speed compared to the LUT-based SPWM units. The CORDIC algorithm has also been applied in [43] for the development of an integrated circuit performing the generation of a 5-kHz SPWM wave using 0.18-μm CMOS technology.

In [44], an LUT is used to store the reference sine-wave digital values corresponding to the time instants of the peaks and nadirs of the triangular wave. The width of each pulse is calculated using an equation based on the similarity of the triangles ABC and ADF depicted in Fig. 3(b). This design method has been validated in case of a 1-kHz switching frequency. A similar approach is also proposed in [45].

In [46], the SPWM pulse train is produced by comparing the sinusoidal and triangular signals generated according to the direct digital synthesis (DDS) technique. The comparison is performed using a high-speed analog comparator. The DDS approach is also used in [47] for the development of a digital SPWM generator chip using 0.35-μm CMOS technology. The maximum clock frequency of this chip is 50 MHz. In [48], the SPWM unit is composed of a DSP chip accomplishing the calculation of the widths of the individual pulses comprising the SPWM wave, which communicates through a parallel port with an FPGA-based unit producing the SPWM control signals.

The regular-sampled PWM technique presented in [28], [49], targets to reduce the amount of computation time required in order to facilitate the generation of higher switching frequencies online and in real time. In this technique, the pulse width is calculated once and used over N consecutive switching edges of the SPWM wave pulses. Then, a new sample of the reference sine wave is acquired. Thus, the sampling frequency f_s is reduced by an integer factor of N, resulting in the following relationship with the corresponding carrier frequency f_c:

$$f_s = f_c/N. \tag{2}$$

Consequently, the number of calculations required to produce the complete SPWM waveform is N times less than in the conventional SPWM generation methods.

A common disadvantage of the previously proposed SPWM generators described previously is that they have been designed to operate at low-switching frequencies, f_c (i.e., 1–20 kHz), while their operation at higher switching frequencies has not been explored yet. In this paper, an FPGA-based SPWM generator is presented, which is capable to operate at switching frequencies up to 1 MHz; thus, it is capable to support the high switching frequency requirements of modern single-phase dc/ac power converters. Compared to the past-proposed SPWM generators, in the proposed architecture the values of both the

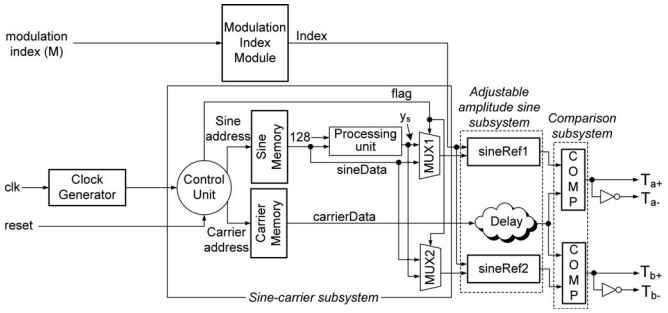


Fig. 4. Architecture of the proposed SPWM generation unit.

reference sine and triangular waves are stored in the FPGA device Block RAMs (BRAMs) in order to exploit their one-clock-cycle access time, thus providing a much higher switching-frequency capability. The proposed design exhibits architectural flexibility features, enabling the change of the SPWM switching frequency and modulation index either internally, or externally. The proposed SPWM unit has been implemented in a single chip in order to enable the reduction of the complexity, cost, and development time of the dc/ac inverter control unit.

The architecture of the proposed FPGA-based SPWM generator is analyzed in Section II, and the simulation and experimental results are presented in Section III. Finally, the performance of the FPGA generator presented in this paper is compared to that of the past-proposed systems, and the corresponding results are analyzed in Section IV.

II. Proposed SPWM Generator

The architecture of the proposed SPWM generation unit is presented in Fig. 4. The system inputs are the modulation index of the output SPWM wave M in single precision floating point arithmetic ranging from 0 to 1, as well as the "clock" and "reset" signals.

The architecture of the proposed system has been built using 8-bit fixed-point arithmetic and it consists of five subsystems, which implement the SPWM generation algorithm. The values of a sinusoidal wave, mathematically being in the range $[-1, 1]$, have been adapted in the proposed architecture to the equivalent range of [0, 255] with the zero point corresponding to the discrete value of "128."

A. Clock Generator Subsystem

The "Clock generator" subsystem takes as input the FPGA input clock and produces a new clock signal used by the digital circuits of the proposed SPWM generator, such that the desired SPWM switching frequency f_c specified by the designer/user is generated. A two-state finite state machine (FSM) is initially used to set the input clock frequency $f_{\rm clk}$ to $f_{\rm clk}/2$ and then a Digital Clock Manager module adapts this frequency to the desired value. The Very high speed integrated circuit Hardware Description Language (VHDL) code of the DCM module is illustrated in Fig. 5. The FSM is kept constant for every different switching frequency, while only the operational parameters "CLKFX_MULTIPLY" and "CLKFX_DIVIDE" of the DCM

```
clkgen: DCM
Generic Map (
                CLKFX_MULTIPLY => 2,
                CLKFX_DIVIDE   => 1
)
PORT MAP (
                clkin => clk,
                clkfb =>sysclkfb,
                rst   =>'0',
                clk0  => sysclk,
                clkfx =>sysclkx2
);
buf : BUFG port map (
                              I  =>sysclk,
                              O =>sysclkfb
);
FSM_label:  FSM port map (
                                    clk     => sysclkx2,
                                     output => new_clock
);
```

Fig. 5. VHDL code of the DCM module in the "Clock generator" subsystem.

module are changed according to the switching frequency requirements of the SPWM output waveform. Thus, the proposed SPWM generator is flexible to be adapted to the generation of any operating switching frequency specified by the system designer/user.

B. Modulation Index Subsystem

The "Modulation index" subsystem is used to convert the floating-point modulation index M, which is input in the proposed SPWM generation system $(M \in [0,\ 1])$ to the corresponding value in fixed-point arithmetic.

Initially, the value of M is transformed into a new floating point value y_M according to the following equation:

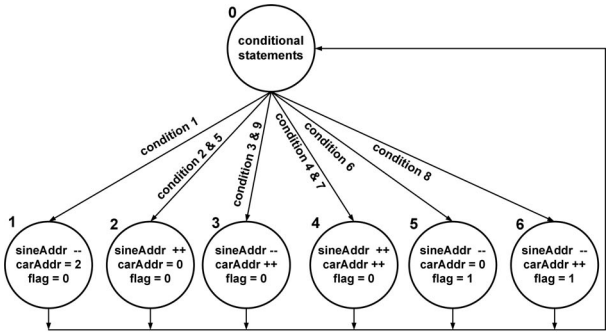
$$y_M = M \cdot (2^{n-1} - 1) + 2^{n-1} \tag{3}$$

where n is the digital word length of the architecture.

Increasing the value of n enables to control the modulation index of the generated SPWM wave with higher resolution, but also results in higher requirements for FPGA device resources. The floating point value produced is then converted into a fixed-point value ranging from 0 to 255, via a float-to-fixed point conversion unit, thus producing the "*Index*" output of the "Modulation index" subsystem depicted in Fig. 4.

C. Sine-Carrier Subsystem

The "Sine-Carrier" subsystem consists of the control unit, two BRAMs, which contain samples of the sinusoidal and triangular (i.e., carrier) waves and two multiplexers that produce the two constant-amplitude reference sine waves used for the production of the SPWM output signals. The BRAMs of the sine wave and carrier operate as LUTs. Both the sinusoidal and triangular waves are sampled and quantized with the same sampling frequency f_s using MATLAB (e.g., $f_s = 4$, 8 MHz, etc.). In order to minimize the utilization of the FPGA resources, only the values of the first quarter of the constant-amplitude



(a)

Condition 1: if carAddr = end && sineAddr = end
goto 1
Condition 2: elsif carAddr = end && sineAddr != end
goto 2
Condition 3: elsif carAddr != end && sineAddr = end
goto 3
Condition 4: elsif carAddr != end && sineAddr != end
goto 4
Condition 5: elsif carAddr = end && sineAddr = start
goto 2
Condition 6: elsif carAddr = end && sineAddr = 1
goto 5
Condition 7: elsif carAddr != end && sineAddr = start
goto 4
Condition 8: elsif carAddr = !end && sineAddr = 1
goto 6
Condition 9: else
goto 3

(b)

Fig. 6. FSM of the control unit in the proposed SPWM generator: (a) flowchart and (b) pseudocode of the conditional statements.

sine-wave period (i.e., during the time interval $0 - \pi/2$) are stored in the corresponding BRAM, while the values of the sine wave during the time interval $\pi/2 - 2\pi$ are calculated by mirroring and inverting the values of the first quarter. The BRAM of the carrier contains the values of a complete period of the reference triangular wave. Consecutive addresses of both memories ("Sine address" and "Carrier address," respectively, in Fig. 4) are generated in every clock cycle by the control unit. The control unit also produces a "flag" signal, which is responsible for the retrieval of the sine-wave values during the time interval $\pi - 2\pi$ of the reference sine-wave period. The BRAM of the constant-amplitude sinusoidal wave is scanned up and down four times, since this memory contains only the values during the first quarter of the sinusoidal-wave period, as analyzed previously. The FSM generating the addresses of the sinusoidal and carrier memory pointers, "sineAddr" and "carAddr," respectively, is depicted in Fig. 6(a). The first state of this FSM (i.e., "State 0") contains all possible conditions of the memory address pointers, which are listed in the pseudocode illustrated in Fig. 6(b). The value of the "flag" signal determines the up or down direction of consecutive accesses performed for retrieving the data stored in the BRAM memory of the reference sine wave. While "flag" is set to 0, the multiplexer "MUX1" outputs the data read from the constant-amplitude sinusoidal memory ("sineData" in Fig. 4). Otherwise, "MUX1" outputs the values corresponding to the second half-cycle (i.e., during $\pi - 2\pi$) of the constant-amplitude sinusoidal wave (parameter "y_s" in Fig. 4).

These values are produced by the processing unit of the "Sine-carrier subsystem" by converting the positive values stored in the sinusoidal memory to the corresponding negative values, according to the following equation:

$$y_s = x - [(x - 2^{n-1}) \times 2] \tag{4}$$

where x is the positive value stored in the BRAM of the sine wave.

The multiplexer "MUX2" in Fig. 4 is used for the production of the second constant-amplitude reference sine wave, which operates with a 180° phase difference compared with the one analyzed above.

D. Adjustable Amplitude Sine Subsystem

The "Adjustable amplitude sine" subsystem takes as input the constant-amplitude reference sinusoidal values produced by the "Sine-Carrier" subsystem and generates a sinusoidal digital signal y_a with an amplitude adjustable according to the value of the modulation index M which is an input in the proposed SPWM generation system. The value of y_a is in the range 0–255 and it is calculated as follows:

$$y_a = \frac{(y - 2^{n-1}) \times (\text{Index} - 2^{n-1})}{(2^{n-1} - 1)} + 2^{n-1} \tag{5}$$

where y is the value of the constant-amplitude reference sine wave and *Index* is the output of the "Modulation Index" subsystem, described in Section II-B.

E. Comparison Subsystem

The "Comparison" subsystem implements the comparison between the high-frequency constant-amplitude triangular wave (carrier) with the two low-frequency reference sine waves, using two comparators ("COMP" in Fig. 4). The control signals T_{a+}, T_{a-}, T_{b+}, and T_{b-} of the single-phase dc/ac inverter power switches depicted in Fig. 1 are generated from the outputs of the corresponding comparators of this subsystem, thus forming the SPWM wave (V_{spwm} in Figs. 1 and 2) at the dc/ac inverter output terminals. The outputs of the comparators in the "Comparison" subsystem (i.e., control signals T_{a+} and T_{b+}) are equal to one when the corresponding output of the "Adjustable amplitude sine" subsystem described in Section II-C is equal to or greater than the current digital value of the carrier signal. The DC/AC inverter control signals T_{a-} and T_{b-} are produced by inverting T_{a+} and T_{b+}, respectively.

III. Validation and Performance Evaluation

The performance of the proposed FPGA-based SPWM generator has been evaluated on an actual design, which has been fully implemented and downloaded to an FPGA board. The digital word length of the implemented architecture has been set equal to $n = 8$, while the frequency of the reference sine waves

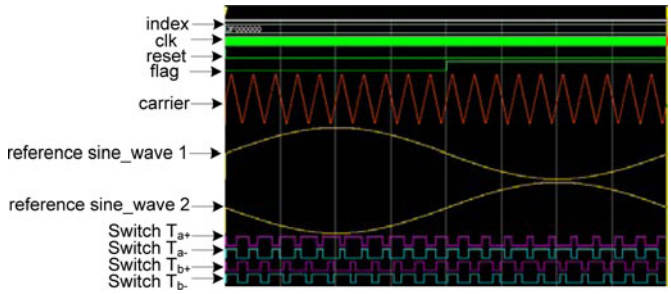


Fig. 7. Major internal signals of the proposed system and the SPWM outputs generated in case that $f_c = 1$ kHz, $f_s = 4$ MHz, and $M = 0.5$.

is 50 Hz. Several simulation and experimental tests were performed in order to verify the correct operation of the proposed SPWM generator and quantify its ability to accurately produce the desired SPWM waveforms. As analyzed next, the results of this evaluation process are universal, independently from the type of the target single-phase dc/ac inverter application, where the proposed system will be incorporated. The simulation and experimental results presented in this section demonstrate the ability of the proposed SPWM generator to operate over a wide range of switching frequencies (1 kHz–1 MHz) and modulation index values (0–1) in single-phase dc/ac inverter applications.

A. System Validation by Simulation

The architecture presented in the previous section has been synthesized using the VHDL language and its correct operation has been verified at both low- and high-carrier frequency levels using the ModelSim 6.3f simulator. The major internal signals of the proposed system and the SPWM outputs in case that $f_c = 1$ kHz, $f_s = 4$ MHz, and $M = 0.5$ are plotted in Fig. 7. A low-carrier frequency has been used in this example only for demonstration purposes, since it enables the easy discrimination of all SPWM pulses produced within a period of the reference sine wave and the observation of their width.

As analyzed in Section II, the SPWM output is generated at the intersection of the sinusoidal and triangular waveforms at certain sampling instants. When the value of each sine wave is higher than the triangular wave value, the output pulse is set to logical "1," else it is set to logical "0."

B. Experimental Results

A laboratory prototype of the proposed FPGA-based SPWM generation system (see Fig. 4) was implemented using the commercially available XILINX XUPV5-LX110T development board for downloading the implemented SPWM design, which contains the XC5VLX110T Virtex-5FPGA device. The proposed SPWM generator is suitable for incorporation in single-phase dc/ac inverter applications and as an example, the experimental, oscilloscope measurements of the T_{a+} SPWM control signal (T_{a-}, T_{b+}, and T_{b-} exhibit similar patterns) in case that $f_c = 1$ kHz and $f_c = 1$ MHz, respectively, are illustrated in Fig. 8. Using a 1-MHz carrier frequency, results in 20 000 pulses spread over the 1/50 Hz time period of the T_{a+} signal. Thus, in order to enable the visibility of the individual SPWM pulses,

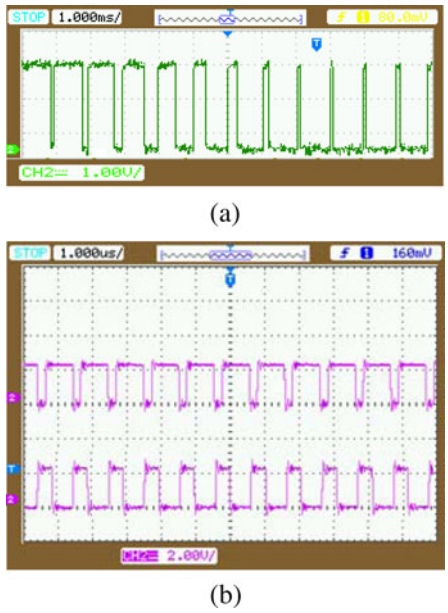


Fig. 8. Oscilloscope measurements of the T_{a+} SPWM control signal: (a) $f_c = 1$ kHz, $f_s = 4$ MHz, and $M = 0.9$ and (b) $f_c = 1$ MHz, $f_s = 32$ MHz, and $M = 0.5$.

two different portions of this signal are illustrated separately in the upper and lower waveforms, respectively, which are plotted in Fig. 8(b).

Then, a unity-gain differential amplifier was used in order to subtract the T_{a+} and T_{b+} control signals generated by the proposed SPWM generation system (see Fig. 4), thus producing a wave equivalent to the output SPWM signal of a single-phase dc/ac inverter, V_{spwm} in Figs. 1 and 2. This hardware-emulation process has the advantage of low cost, since building an actual power stage of a single-phase dc/ac inverter (including power switches, drivers, etc.) is avoided. Additionally, it enables to evaluate the performance of the proposed SPWM generator without being affected by nonidealities of an experimental prototype dc/ac power inverter (e.g., dead-time effect, power switch finite turn-on, and turn-off times, etc.), which depend on the exact type of the dc/ac inverter application comprising the proposed SPWM generator and deteriorate the quality of the generated SPWM signal [5]. The minimization of the impact of such effects is performed during the design process of the dc/ac inverter; thus, the investigation of their impact on the quality of the SPWM output voltage of the dc/ac inverter is not within the scope of this paper. The hardware-emulation process described previously has been applied in order to experimentally evaluate the performance of both the new SPWM generator presented in this paper, as well as that of the past-proposed SPWM generation units. The corresponding experimental results are presented in the following paragraphs of this paper.

The Fast Fourier Transforms (FFTs) of the experimentally measured SPWM output waveforms, which are produced by the hardware emulation process described previously, in case that the SPWM switching frequency f_c is 1 kHz and 1 MHz are illustrated in Fig. 9(a) and (b), respectively. It is observed that, as expected due to the attributes of the unipolar SPWM

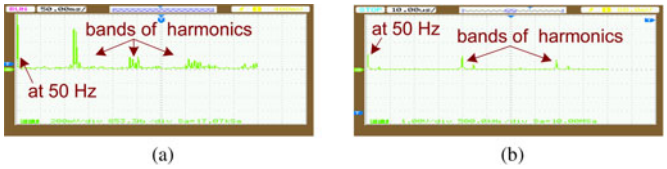


Fig. 9. FFT of the experimentally measured unipolar SPWM output waveform for single-phase applications: (a) $f_c = 1$ kHz, $f_s = 4$ MHz, and $M = 0.9$ and (b) $f_c = 1$ MHz, $f_s = 32$ MHz, and $M = 0.5$.

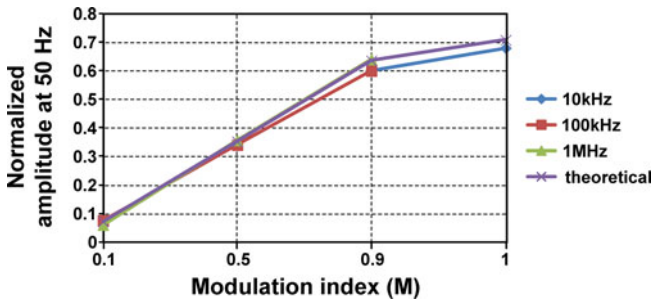


Fig. 10. Normalized experimental and theoretical amplitude at 50 Hz of the generated SPWM waveform using the proposed SPWM generator for $f_s = 4$ MHz, $M = 0.1 - 1$, and $f_c = 10$ kHz $-$ 1 MHz.

technique, the generated SPWM signal consists of the fundamental at 50 Hz, while the harmonics appear as sidebands at multiples of twice the switching frequency. These experimental results also confirm the correct operation of the proposed SPWM generator at high switching frequency (i.e., up to 1 MHz).

The experimentally measured and theoretically calculated amplitude of the generated SPWM waveform at the fundamental frequency (i.e., 50 Hz), both normalized over the amplitude of the SPWM pulses [i.e., V_d in (1) and Fig. 2], for $f_s = 4$ MHz, $M = 0.1 - 1$, and $f_c = 10$ kHz $-$ 1 MHz are displayed in Fig. 10. The deviation $\Delta V\,(\%)$ between the experimental and theoretical amplitudes of the generated SPWM waveform at the fundamental frequency has been calculated as follows:

$$\Delta V(\%) = \frac{|\text{theoretical} - \text{experimental}|}{\text{theoretical}} \cdot 100\%. \qquad (6)$$

The average value of $\Delta V\,(\%)$ over the 0.1–1 range of the modulation index, in each switching frequency, is 3.9–6.8%. Thus, it is verified that using the proposed SPWM generator the amplitude of the sinusoidal wave at the output of a single-phase dc/ac inverter can be controlled with high accuracy.

C. Power Consumption and System Resources

A post place-and-route analysis of the implemented system has been performed using the XILINX ISE Design Suite 10.1 software. The dynamic, quiescent, and total power consumption of the FPGA device in the post place-and-route implementation of the proposed system have been derived using the power analyzer of the XILINX ISE Design Suite 10.1 software and they are plotted in Fig. 11 as a function of f_c/f_s.

The total power consumption at the 1 / 64 MHz upper end is 6.1% higher compared to that at 10 kHz/4 MHz. Depending

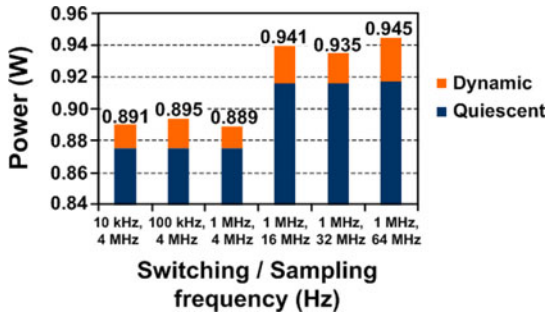


Fig. 11. Power consumption of the proposed SPWM generation system for various values of f_c/f_s, in case of the XC5VLX110T Virtex-5 XILINX FPGA device.

on the values of f_c and f_s, 97.04–98.43% of the total power consumption corresponds to the quiescent power, while the rest is consumed during dynamic operating conditions.

The resources required for the implementation of the full system are presented in Table I for various combinations of the sampling and carrier frequencies f_s and f_c respectively. The corresponding maximum operating clock frequency values are shown in the last row of Table I. It is observed that the proposed design is capable to operate at switching frequency values up to 1 MHz, thus covering the requirements of modern high-switching-frequency single-phase dc/ac power converters, as analyzed in Section I.

Also, a low percentage of the FPGA device logic and memory blocks are occupied by the proposed SPWM generation architecture enabling the implementation of additional dc/ac inverter control algorithms in the same FPGA IC (e.g., for regulating the dc/ac inverter output voltage, current or frequency to the desired value, etc.).

Increasing the sampling frequency f_s results in a more accurate calculation of the widths of the individual SPWM pulses, but, as shown in Table I, the BRAM memory requirements for the implementation of the LUTs described in Section II-C for the sinusoidal and carrier waves are also increased. Additional tests performed for higher sampling frequencies indicated that the BRAMs are the critical resource that restricts further increase of the sampling frequency (e.g., to 128, 256 MHz, etc.).

IV. Performance Comparison With the Past-Proposed SPWM Generators

In order to compare their performance with that of the SPWM generation unit, which is presented in this paper, the major past-proposed SPWM generation methods were also implemented and evaluated using simulation and experimental tests and the corresponding results are presented in this section. The systems developed are those based on the past-proposed techniques that implement the triangular wave using an up-down counter, and the sampled reference sinusoidal wave is stored in digital format in an LUT implemented in the FPGA internal memory [28], [38], [41], [49]. The reference sine wave is sampled at the time instants corresponding to either the nadirs, peaks, both at the nadirs and the peaks of the carrier wave or with one sample per $N = 3$ carrier cycles (undersampling), as analyzed

TABLE I
FPGA RESOURCES REQUIRED BY THE PROPOSED SPWM ARCHITECTURE FOR VARIOUS VALUES OF f_c AND f_s

f_c / f_s	1kHz / 4MHz	100kHz / 4MHz	500kHz / 4MHz	1MHz / 4MHz	100kHz / 16MHz	500kHz / 16MHz	1MHz / 16MHz	100kHz / 64MHz	500kHz / 64MHz	1MHz / 64MHz
DSPs	6 / 64 (9%)	6 / 64 (9%)	6 / 64 (9%)	6 / 64 (9%)	6 / 64 (9%)	6 / 64 (9%)	6 / 64 (9%)	6 / 64 (9%)	6 / 64 (9%)	6 /64 (9%)
Slice Registers	3447 / 69120 (4%)	3441 / 69120 (4%)	3438 / 69120 (4%)	3437 / 69120 (4%)	3445 / 69120 (4%)	3442 / 69120 (4%)	3441 / 69120 (4%)	3454 / 69120 (4%)	3451 / 69120 (4%)	3450 / 69120 (4%)
Slice LUTs	2860 / 69120 (4%)	2843 / 69120 (4%)	2838 / 69120 (4%)	2840 / 69120 (4%)	2852 / 69120 (4%)	2846 / 69120 (4%)	2846 / 69120 (4%)	2901 / 69120 (4%)	2893 / 69120 (4%)	2893 / 69120 (4%)
BRAMs	6 / 148 (4%)	6 / 148 (4%)	6 / 148 (4%)	6 / 148 (4%)	21 / 148 (14%)	21 / 148 (14%)	21 / 148 (14%)	79 / 148 (52%)	79 / 148 (52%)	79 / 148 (52%)
max. clock frequency	158MHz	155MHz	144MHz	149MHz	126MHz	138MHz	131MHz	96MHz	97MHz	99MHz

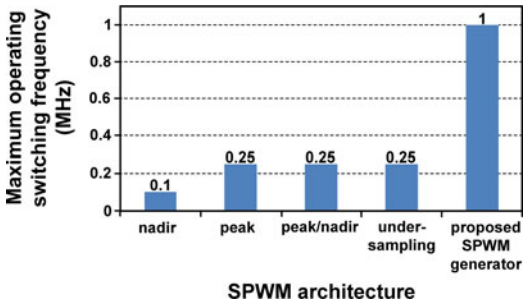


Fig. 12. Experimentally measured maximum operating switching frequency of the SPWM architectures under study.

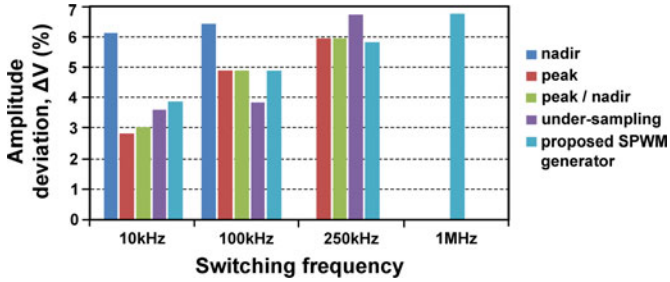


Fig. 13. Average deviation for $M = 0.1 - 1$ between the experimental and theoretical amplitude at 50 Hz in the SPWM waveform generated by each of the SPWM architectures under study at various switching frequencies.

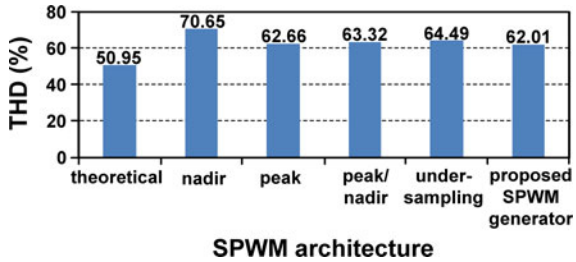


Fig. 14. Experimentally measured THD of the SPWM waveform produced by each architecture under study and the THD of the corresponding theoretical SPWM waveform, in case that $f_c = 1$ kHz and $M = 0.9$.

in Section I. These architectures were adapted such that they produce a unipolar SPWM output for single-phase full-bridge dc/ac inverters, in order to be fully compatible with the new SPWM generator proposed in this paper. Both the newly and the past-proposed SPWM generator architectures were fully implemented on the XC5VLX110T Virtex-5 XILINX FPGA device.

The maximum possible operating switching frequency that can be achieved by each of the SPWM generation architectures has been experimentally measured and it is presented in Fig. 12. It is observed that compared to the past-proposed architectures, the SPWM generation unit proposed in this paper is capable to operate at a much higher maximum switching frequency.

The average deviation $\Delta V\,(\%)$ for $M = 0.1 - 1$ between the experimentally measured and the theoretically calculated amplitude of the fundamental frequency (i.e., 50 Hz) in the SPWM waveform generated by each of the SPWM architectures under study at various switching frequencies is depicted in Fig. 13. Except the sampling-at-nadir design, the rest of the architectures obtain similar performance in each switching frequency. However, only the proposed method is capable to operate up to 1 MHz and simultaneously retain the high-accuracy feature of the generated SPWM output signal. The SPWM generation method based on the triangles similarity [44], [45] was also implemented initially, but the resulting average value of $\Delta V = 66\%$ for a 10-kHz switching frequency was considered unacceptably high. Thus, the operation of this SPWM technique at higher switching frequencies was not further investigated.

An additional metric used to investigate the quality of the generated SPWM waveform is the Total Harmonic Distortion (THD) that is defined as follows [5]:

$$\text{THD}\ (\%) = \frac{\sqrt{\sum_{h\neq 1} V_h^2}}{V_1} \cdot 100\ \% \tag{7}$$

where V_1 (V) is the RMS value of the fundamental (e.g., 50 Hz) and V_h (V) is the RMS value of the hth harmonic of the SPWM signal.

The experimentally measured THD (%) of the SPWM waveform produced by each architecture under study for $f_c = 1$ kHz and $M = 0.9$ and the THD of the corresponding theoretical SPWM waveform, which is used as a reference, are presented in Fig. 14. A low switching frequency has been applied in order to adapt to the low-input-signal bandwidth specifications of the laboratory instrument used to perform these measurements (HAMEG HM8027 distortion meter). It is observed that the

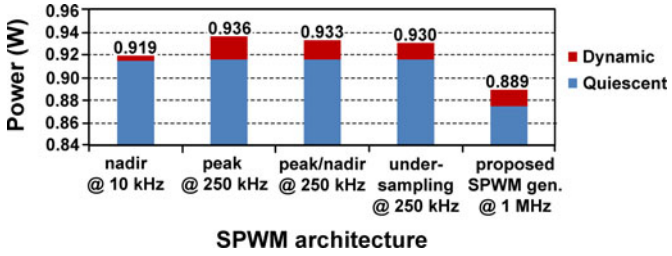


Fig. 15. Total power consumption of the SPWM generator architectures at their maximum operating switching frequency.

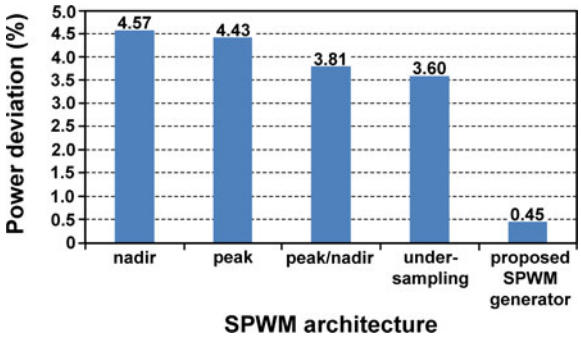


Fig. 16. Average deviation of the power consumption when operating at switching frequencies lower than the maximum possible switching frequency of each SPWM generation architecture.

THD (%) of the SPWM signal produced by the proposed SPWM generator deviates from the THD of the corresponding theoretical SPWM waveform by 11.06%, while the past-proposed architectures deviate by 11.71–19.69%. Thus, the SPWM waveform produced using the proposed system achieves a more accurate representation of the desired SPWM wave.

The dynamic, quiescent, and total power consumption of the FPGA device for each of the post place-and-route implementations of all SPWM generator architectures under study, when operating at their maximum possible switching frequency, have been derived using the power analyzer of the XILINX ISE Design Suite 10.1 software and they are displayed in Fig. 15. The total power consumption of the proposed architecture, although it operates at its 1-MHz maximum switching frequency, is less than that of the past-proposed SPWM generation systems by 3.26–5.02%.

In order to investigate the variability of the power consumed by each of the SPWM generation architectures when operating at switching frequencies lower than the maximum possible operating switching frequency, the corresponding average deviations are illustrated in Fig. 16. The proposed architecture exhibits the highest stability in terms of this power consumption, thus indicating its suitability for incorporation in a wide range of single-phase dc/ac inverter applications with different switching frequency requirements.

In terms of the FPGA resources required, all SPWM generator architectures occupy a small fraction (≈9%) of the medium-sized FPGA device used. The BRAMs are the critical resource that restricts further increase of the sampling frequency of the SPWM generator proposed in this paper. The next critical resources are the DSPs that occupy 3% more space in the FPGA device of the proposed SPWM generator.

V. Conclusion

The SPWM principle is widely used in dc/ac inverters in energy conversion and motor drive applications. The past-proposed SPWM generators have been designed to operate at low switching frequencies (i.e., 1–20 kHz), while their operation at higher switching frequencies had not been explored so far.

In this paper, an FPGA-based SPWM generator has been presented, which is capable to operate at switching frequencies up to 1 MHz, thus it is able to support the high switching frequency requirements of modern single-phase dc/ac inverters. The proposed design occupies a small fraction of a medium-sized FPGA and, thus, can be incorporated in larger designs, while it has a flexible architecture can be adapted to a variety of single-phase dc/ac inverter applications. Both post place and route simulation results and experimental verification results on actual hardware were presented, demonstrating the successful operation of the proposed SPWM generator at high switching frequencies.

The past-proposed SPWM generation techniques were also implemented and their performance was compared to that of the new architecture presented in this paper. The postlayout simulation and experimental results confirm that the proposed SPWM generator exhibits much faster switching frequency, lower power consumption, and higher accuracy of generating the desired SPWM waveform.

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