A NEW METHOD FOR THE DESIGN OF A CLASS-D DC TO AC INVERTER

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ABSTRACT

A new design for a generalized DC to AC inverter is proposed, based on the class-D operation scheme and employing the SPWM technique. The inverter is built around a MOSFET bridge whose one side operates at high frequency, while the other operates at 50Hz thus reducing the overall cost. The unit operates over a wide DC input range and delivers an approximately constant efficiency from 25% to 100% load, low output impedance, low THD and excellent transient stability. The state-space model of the inverter is used for the tuning procedure. Experimental results under various loading conditions are given and verify theoretical expectations.

INTRODUCTION

Recently, many solutions have been proposed for the design and implementation of efficient inverters [1-4]. A good inverter behaves as a sinusoidal voltage source with low internal resistance and low output voltage variations with DC input voltage. Usually these characteristics are badly affected by the required networks for class-D operation and by the presence of strong high-order harmonics produced by pulse modulators.

Most of the proposed methods for inverter design are microcomputer-based systems developed for specific applications. However, at light loads, these inverters have poor efficiency because of the quiescent power consumed and because most of them do not use MOSFETs [5]. MOSFETs require low control power and could be more efficient compared to bipolar devices. Moreover, in the "ON" state, MOSFETs have no saturation voltage but a small "ON" resistance in forward and reverse drain-source biasing.

This paper describes a new design of a Class D inverter which operates over a wide DC input range (-20% to +100%) and attains approximately constant efficiency (about 80% in the range from 25% to 100% full load). This is accomplished by using low "ON" resistance MOSFETs, low-power consumption stages and two specially-designed feedback loops. The analog control circuitry is simple and efficient and the use of logic gates for pulse processing makes digital system interface easier. The proposed design offers low internal resistance and low-distortion output voltage. Although no special components are used, the inverter does not lack any features offered by more complex systems.

DESCRIPTION

The block diagram of the proposed design, shown in Fig. 1, consists of: (a) a low distortion, constant amplitude, sinewave source, (b) a power SPWM modulator with constant gain, (c) a combination of a lowpass LC filter and a step-up transformer and (d) an optional output LC lowpass filter (EMI).

The sinewave source consists of: (i) a 50 Hz square wave generator that drives a CMOS gate powered by a constant DC voltage supply producing a constant-amplitude output square wave and (ii) a high-Q bandpass filter with flat response [6], resulting in a high-quality sinewave used as a reference signal to drive the rest of the circuitry which is essentially a power amplifier.

At low frequencies, the linearity of a modulator that contains a power stage depends on the type of modulation used, the DC supply voltage and the dead-time effect [7]. In case of feedback, the linearity also depends on the residual high-frequency components used in modulation. The power stage internal resistance reduces the output voltage amplitude and increases the losses at high output current levels. Inside the modulator two PWM signals are produced [8] which are combined to give two new signals, one high-frequency carrier and a low frequency 50 Hz modulated signal, as shown in Fig. 2. Those two new signals drive a bridge power stage because their difference is an SPWM signal. For this reason, only one side of the bridge operates at high frequency, while the other side operates at 50 Hz and thus may use lower-frequency components without any significant sacrifice, but resulting in much lower cost. In the proposed implementation, the power bridge uses n-channel MOSFETs and the 50 Hz side and its drive are simpler. The power modulator has constant gain independent of DC input voltage variations, because the triangular wave used to produce the PWM signals has an amplitude proportional to the DC input voltage. An additional stage may be used to eliminate distortion due to dead-time effects, but this is not always necessary because the use of negative feedback minimizes this kind of distortion. The fed-back high-frequency components will not substantially affect the modulator gain, if their maximum amplitude is kept at very low levels compared to the triangular wave.

A low value of L is chosen in the LC lowpass filter in order to keep low the output impedance at 50 Hz. This is usually easily done, because the LC filter is tuned at a much higher frequency. The step-up transformer is an ordinary low-loss toroidal type.

The proposed system is controlled by two minimum-time loops [9], an internal and an external. The internal loop controls only the power modulator subsystem thus reducing system errors. The power stage internal resistance in combination with the transformer and the LC network form a band elimination filter. Under capacitive load, the overall center frequency is lowered and thus the maximum capacitive load determines the feedback frequency response. The internal-loop pole is placed such that it compensates for any phase shift instabilities. From the above it follows that inductive loads cannot affect the stability of the system. Since the loop is of a minimum-time control type, the modulator frequency response is not affected, but its linearity is improved at low frequencies. The lowest frequency for the compensation pole is 50 Hz, since below that frequency there is no need to further reduce the modulator output resistance. The feedback pulses that appear at the modulator input are demodulated by the compensation pole of the internal loop.

The internal loop and the LC network have a frequency response determined by the two LC network poles. Therefore, the external loop compensation pole may be placed near 50 Hz and the feedback voltage gain can be set equal to unity at a frequency which lies sufficiently before the first expected pole, under any expected load. The placement of a zero at the external loop maintains the gain at unity level thus reducing the errors. This zero-pole cancellation further improves the characteristics of the system under low loading conditions. An additional decoupling zero near 50 Hz must be placed in the external loop in order to avoid transformer saturation and cause instability problems.

An optional EMI filter may be connected at the output tuned at a higher frequency than the demodulating LC frequency and give a very clean sinewave at the output. This filter must be taken into account in the stability analysis of the system and will increase the time response under transient conditions.

STABILITY ANALYSIS

The optimization of the inverter stability is based on a simulation approach of the main characteristics of the circuit. The

internal structure of many stages is fixed and does not play an important role in the stability of the inverter. On the other hand, some of the components form the dominating zeros and poles of the system, so they prescribe the transient performance. The block diagram for the simulation of the circuit is illustrated in Fig. 3.

The subsystems are treated as blocks characterized by their main behavior (i.e. gain and time delay). The crucial components (RC, RL and RLC combinations, transformer etc.) are modeled in detail. A generic load (in the shaded box) is supposed to be supplied by the inverter. The node voltages and currents of the system are used to formulate the state space model, which is employed for the inverter stability study that follows.

The state equations of the system of Fig. 3 are given below :

$$\frac{dx_1}{dt} = \frac{1}{R_1(R_2+R_3)C_1}\left[-R_1x_1 + R_2(x_8-u) + R_2R_3C_1\left(\frac{dx_8}{dt} - \frac{du}{dt}\right)\right]$$

$$\frac{dx_2}{dt} = \frac{1}{(R_4+R_5)C_2}\left[-x_2 + u + R_5C_2\frac{du}{dt} + R_4C_2\frac{dx_1}{dt}\right]$$

$$\frac{dx_3}{dt} = \frac{1}{C_3}\left[-\frac{x_3}{R_7} + \frac{2x_2 - A_2u_2}{R_6}\right]$$

$$\frac{dx_4}{dt} = \frac{1}{D}\left[L_{22}(u_2 - R_9x_4) - Mx_6\right]$$

$$\frac{dx_5}{dt} = \frac{1}{D}\left[M(u_2 - R_9Mx_4) - (L_{11}+L_1)x_6\right]$$

$$\frac{dx_6}{dt} = \frac{1}{C_4}\left[x_5 - x_7\right]$$

$$\frac{dx_7}{dt} = \frac{1}{L_2}\left[x_6 - x_9\right]$$

$$\frac{dx_8}{dt} = \frac{1}{R_{10}R_{12}C_5}\left[-R_{10}x_8 - R_{11}x_6 - R_{11}(R_{10}+R_{12})C_5\frac{dx_6}{dt}\right]$$

$$\frac{dx_9}{dt} = \frac{1}{C_6}\left[x_7 - x_{10}\right]$$

$$\frac{dx_{10}}{dt} = \frac{1}{L_L}\left[x_9 - R_Lx_{10}\right]$$

where :

$$u = V_0\sin(wt) \qquad \frac{du}{dt} = wV_0\cos(wt)$$

$$u_1 = 2x_2 + x_3 \qquad D = (L_{11}+L_1)L_{22} - M^2$$

$$u_2 = A_1u_1 - R_8x_4 = A_1(2x_2 + x_3) - R_8x_4$$

An appropriate computer program was developed for the simulation of the inverter performance, providing the solution of the above equations set. The simulation runs are executed under various load configurations and switching abruptly the load ON and OFF, in order to simulate all possible loading conditions of the inverter. The system component values are adjusted properly so that a smooth and reliable operation is achieved, bounding the transients to a minimum. The resulting element values are used in the construction of the experimental model and the same load behavior is obtained by means of an experimental switching device and various load impedance values. The response of the inverter is very close to the results of the simulation, affected by negligible transients as is reported in the following section.

EXPERIMENTAL RESULTS

An inverter prototype, based on the proposed methodology, was constructed and used to study the real behavior. The values of the components that play an important role in the stability performance were determined as described in the previous section. Various load structures were implemented and connected/disconnected to the inverter output, while voltages, currents and harmonic distortion at specified points of the circuitry were monitored. Some of the experimental results are listed below.

The total harmonic distortion (THD) measured at the output of the inverter without load is 0.44%, while with a 300W resistive load the THD is below 2.2%. These values are very satisfactory. The efficiency of the system, defined as the ratio of output to input power, has a maximum value of 84,1% at 75W and is above 79% for a resistive load of 300W. The fluctuation of the output voltage is maintained in the narrow interval of 221.8 to 222.8V for an input DC voltage range from 20V to 30V giving a DC line regulation of 0.45% which is excellent.

The inverter input and output voltage waveforms are illustrated in Fig. 4. The quality of the output voltage waveform is comparable to the reference input waveform.

The inverter behavior when a slightly inductive load of 75W is connected abruptly to the output is depicted in Fig. 5. The observed transient component on the voltage waveform is negligible and the inverter stability is maintained well within the safety margins.

The same measurement as above, but with an inductive load of 200W, is repeated, and the results are shown in Fig. 6. Again, the stability is guaranteed.

CONCLUSIONS

A Class-D DC to AC inverter was developed based on the proposed design method and was found to operate over a wide DC input range (-20% to +100%) at approximately constant efficiency (about 80%) at light (25%) and at full (100%) load. The inverter had an excellent voltage regulation and low THD. Since the cost of construction is low, the development of such a unit becomes very attractive in a variety of applications, such as stand-alone PV-array supply systems, incorporated in uninterruptible power supply devices, etc.

REFERENCES

1. Manias S., "Power Electronics", 1988 (In Greek).
2. Mohan N., Undeland T. M. and Robbins W. P., "Power Electronics: Converters, Applications and Design", John Wiley and Sons, Inc., New York, 1989.
3. Rashid M.H., "Power Electronics Circuits Devices and theory", Prentice-Hall, Inc., Second Edition, 1993.
4. Bose B.K. "Modern Power Electronics Evolution, Technology, and Applications", IEEE Press, 1991.
5. Pelly Brian R., "Power MOSFETs - A Status Review", March 1983, "Modern Power Electronics Evolution, Technology, and Applications", IEEE Press, p.149,1991
6. Soclof Sidney, "Design and Applications of Analog Integrated Circuits", Prentice-Hall, Inc., Chap. 6, Page 368, 1991.
7. Seung-Gi Jeong and Min-Ho Park, "The Analysis and Compensation of Dead-Time Effects in PWM Inverters", IEEE Trans. on Industrial Electronics, Vol. 38, No. 2, April 1991, p. 108.
8. Mohan N., Undeland T. M. and Robbins W. P., "Power Electronics: Converters, Applications and Design", John Wiley and Sons, Inc., New York, p. 119-120, 1989.
9. Takahashi and Su G. J., "A 500 Hz Power System - Applications", 1989, "Modern Power Electronics Evolution, Technology, and Applications", IEEE Press, p. 582, Fig. 7, 1991.

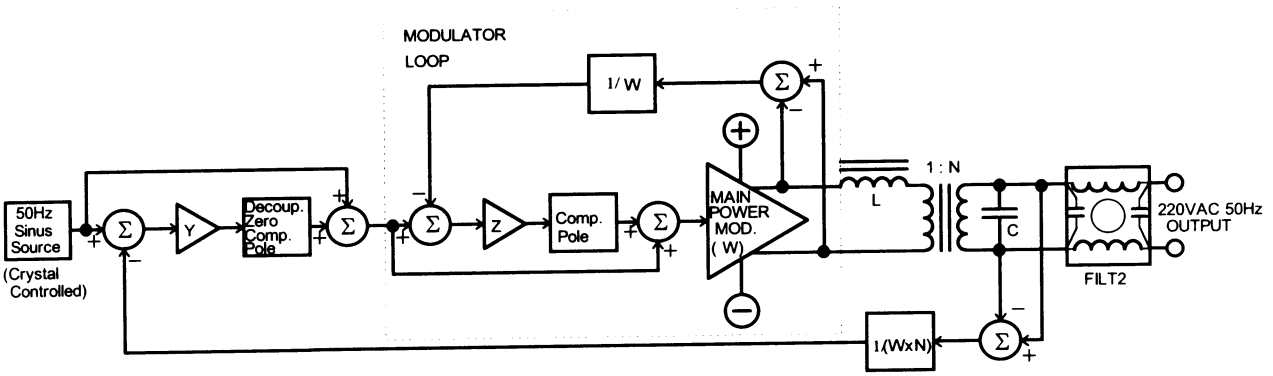
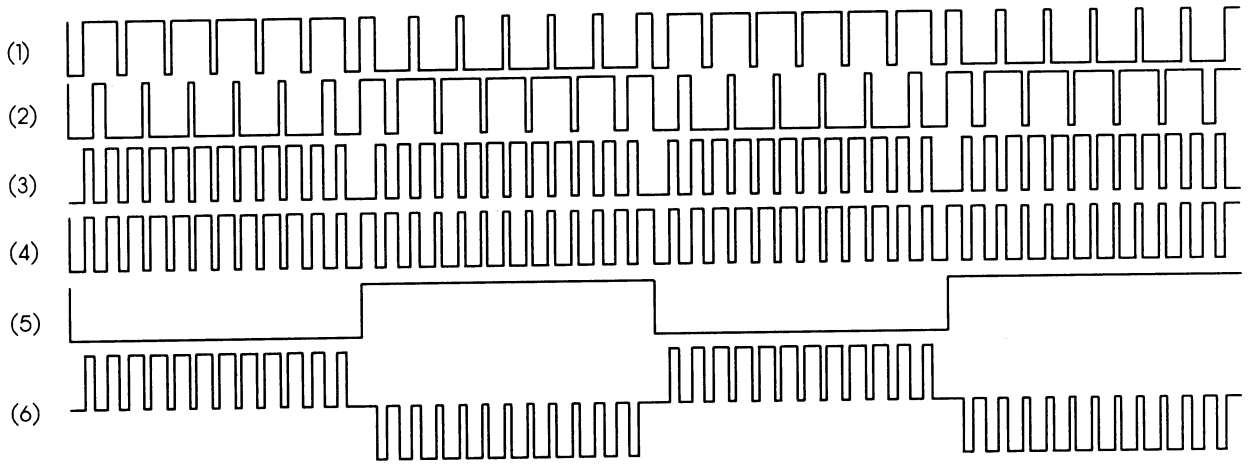


Fig. 1. Block Diagram of the Proposed System



(1). Plain Carrier PWM

(2). Reverse Carrier PWM

(3). (1) EX-OR (2)

(4). (3) EX-OR (5)

(5). Input Sign

(6). SPWM = (1) - (2) = (4) - (5)

Fig. 2. Pulse Waveforms for the Output Drive

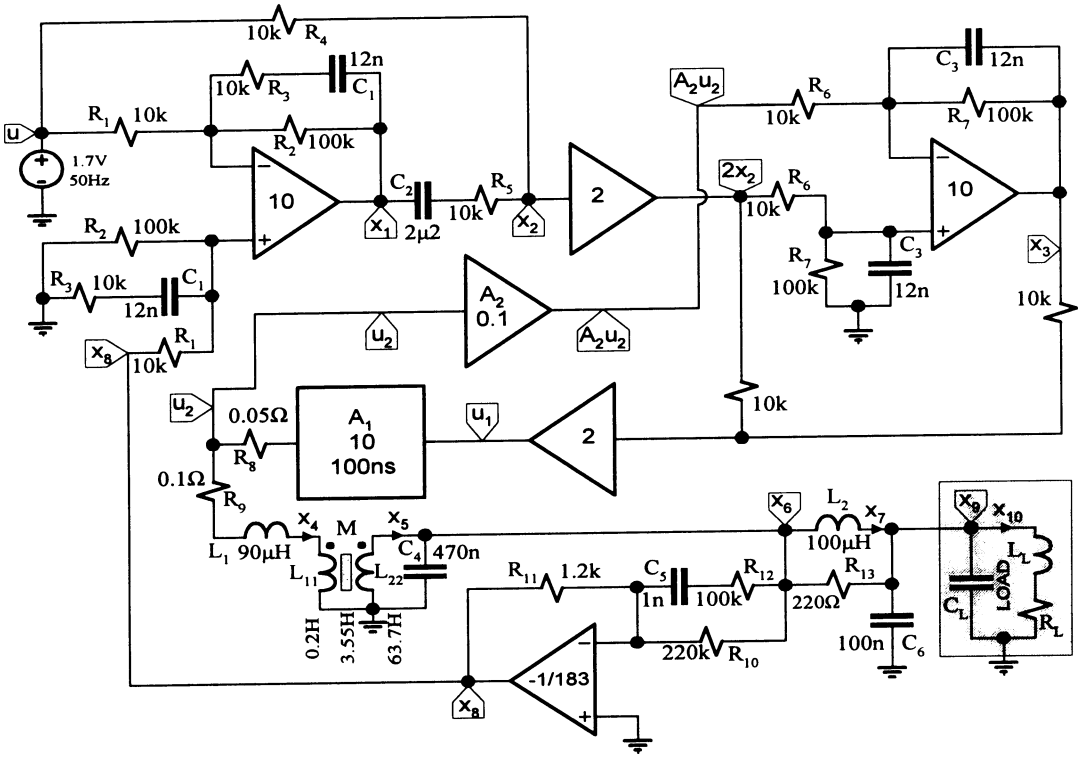


Fig. 3 Inverter Block Diagram Used for Stability Analysis.

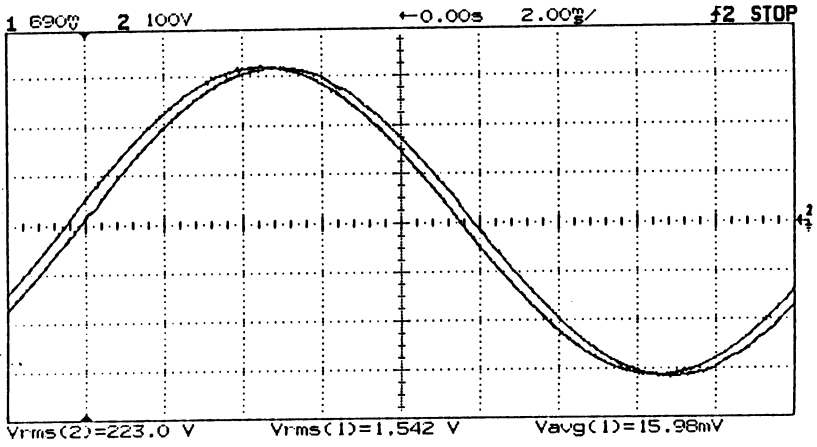


Fig. 4. Comparison of the input (reference) and output waveforms.

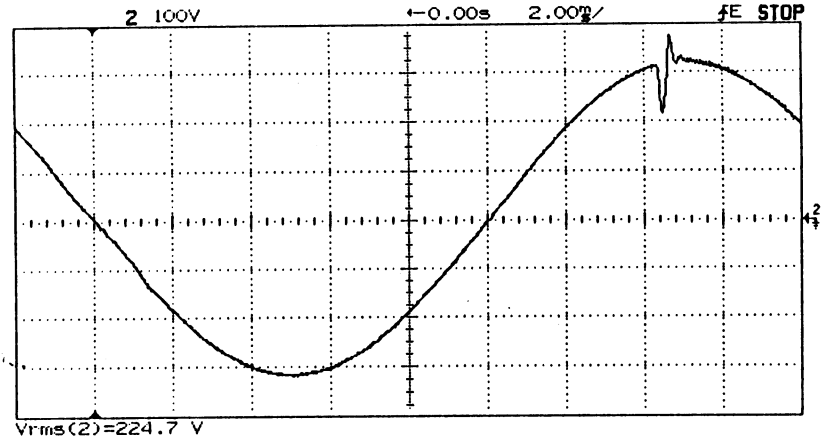


Fig. 5. Transient response with a 75W load burst at the output.

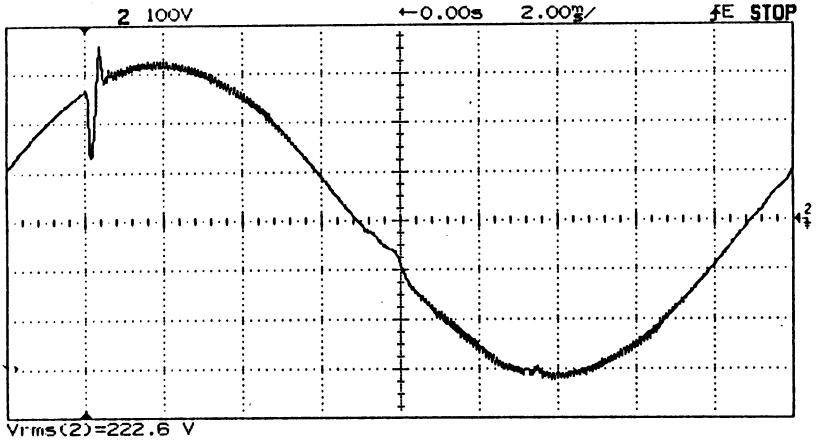


Fig. 6. Transient response with a 200W load burst at the output.

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