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Optimization of SiC-based H5 and Conergy-NPC Transformerless PV Inverters

Stefanos Saridakis Eftichios Koutroulis*
Member, IEEE
School of Electronic and Computer Engineering
Technical University of Crete
Chania, GR-73100, Greece
ssaridakis@isc.tuc.gr efkout@electronics.tuc.gr

Frede Blaabjerg
Fellow, IEEE
Department of Energy Technology
Aalborg University
Aalborg, DK-9220, Denmark
fbl@et.aau.dk

***Abstract* -- The transformerless DC/AC inverters are critical components in the rapidly growing market of grid-connected Photovoltaic (PV) applications. They are synthesized by combining available solutions in terms of the power-section topology, power-semiconductors manufacturing technology and structure of the output filter. Also, the SiC-based power semiconductors are capable to operate reliably at high operating temperature and switching frequency levels combined with a very high efficiency. In this paper, a new design technique is presented for optimizing the switching frequency and structure of the output filter (either LCL- or LLCL-type) in transformerless H5 and Conergy-NPC PV inverters, which employ SiC-type power devices. The design results demonstrate that the optimized SiC-based H5 and Conergy-NPC transformerless PV inverters are more effective in terms of energy production than their non-optimized and Si-based counterparts. Also, by reducing the market price of SiC-type power semiconductors to the level of Si-based power devices, enables the development of optimized SiC-based PV inverters with a lower cost of energy than the corresponding PV inverters based on Si technology, thus maximizing the economic profitability of the PV system.**

***Index Terms* -- Photovoltaic, DC/AC Inverter, Transformerless, Silicon Carbide, Design, Optimization, Genetic Algorithms.**

NOMENCLATURE

C_b	Base capacitance
C_f	Output-filter capacitor
C_t	Total manufacturing cost of the PV inverter
E_i	Total energy injected into the electric grid by the PV inverter during a year
$E(\cdot)$	Switching energy consumption
I_{avg}	Average value of the conduction current of each power switch or diode
I_D	Conduction current of SiC Schottky diodes
$I_{i,avg}$	Average value of the current conducted by the i-th power device
$I_{i,rms}$	RMS value of the current conducted by the i-th power device
$I_o(t)$	RMS value of the current which is injected by the PV inverter into the electric grid
I_R	Peak reverse-recovery current
$I_r(t)$	RMS ripple current conducted by the inverter-side inductor at hour t
I_{rms}	RMS value of the conduction current of each power switch or diode
I_S	Conduction current of SiC JFET power switches
L	Inverter-side inductor of the output-filter
L_b	Base inductance
L_g	Grid-side inductor of the output-filter
L_f	Output-filter inductor
$LCOE$	Levelized Cost Of the Electricity generated
$LCOE_{n-o}$	Cost of electricity of non-optimized PV inverters
$LCOE_{opt}$	Optimal value of the cost of electricity
$LCOE_{Si}$	Cost of electricity of optimized PV inverters comprised of Si-based power semiconductors
P_{cond}	Conduction losses of the SiC-type power semiconductors employed in the power section
P_{cu}	Total power consumption of the control unit
P_d	Power loss on the output-filter damping resistor
$P_{d,\max}$	Maximum power dissipated in the LCL-filter damping resistor during the year
$P_{l,i}(t)$	Total conduction and switching power loss of the i-th power device at hour t
$P_{L,c}$	Core losses of the inductors incorporated in the LCL-type output filter
$P_{L,r}$	Winding losses of the inductors incorporated in the LCL-type output filter
P_o	Power injected into the electric grid
P_{pv}	Maximum Power Point power produced by the PV array
P_{sw}	Switching losses of the SiC-type power

* *Corresponding author.*
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	semiconductors employed in the power section
P_{tot}	Total power loss of the PV inverter
$R_{ac,L}$	High-frequency resistance of the windings of inductor L
R_{ac,L_f}	High-frequency resistance of the winding of inductor L_f
$R_{d,on}$	On-state resistance of the power diode
R_{dr}	Output-filter damping resistor
$R_{s,on}$	On-state resistance of the power switch
$RF_{\max}$	Maximum limit of the ripple factor
RF_{sw}	Ripple factor of the current at the inverter side
S	Diode snappiness factor
SF	Over-sizing factor of the LCL-filter damping resistor
$T_A(t)$	Ambient temperature of the PV inverter at hour t
T_j	Junction temperature of the power semiconductors
$T_{j,i}(t)$	Junction temperature of each SiC-type power semiconductor at each hour t
$T_{j,max}$	Junction-temperature limit for safe operation
V_d	On-state voltage drop across the SiC Schottky diode
V_n	Nominal RMS output voltage of the PV inverter
$V_{pv}(t)$	Output voltage of the PV array at hour t
V_{ref}	Reference (test) voltage
V_s	On-state voltage drop across the SiC JFET power switch
$\boldsymbol{X}$	Vector of the design variables of the optimization process
c_c	Filter capacitor cost per unit capacitance
c_d	Cost of each power diode
c_{hs}	Cost of the heat sink
c_I	Cost per unit inductance of the filter inductors L and L_g
c_{L_f}	Cost per unit inductance of the filter inductor L_f
c_m	Manufacturing cost of the PV inverter without including the cost of the heat sink, power semiconductors and filter components
c_r	LCL-filter damping resistor cost per unit resistance and per unit power
c_s	Cost of each power switch
f	Electric grid frequency
f_{res}	Resonance frequency
f_s	PV inverter switching frequency
$f_{s,\max}$	Maximum permissible switching frequency
$f(\phi, m_a)$	Modulation function of the power semiconductors
m_a	Modulation index of the SPWM voltage produced by the power section of the PV inverter at hour t
n	Total number of power semiconductors comprising the PV inverter power section
n_d	Number of power diodes
n_s	Number of power switches
r_L	Inductor winding low-frequency resistance per unit inductance of [L , L_g]
r_{L_f}	Inductor winding low-frequency resistance per unit inductance of L_f
t	Number of hour
t_{rr}	Reverse-recovery time
Δt	Simulation time-step
θ	Phase angle between the PV inverter output current and the fundamental-frequency component of V_{spwm}
θ_{ca}	Thermal resistance of the heat sink
θ_{jc}	Junction-to-case thermal resistance of the i-th power semiconductor

I. INTRODUCTION

The Photovoltaic (PV) market has been dominated during the last years by the grid-connected PV applications, while, additionally, the installation of single-phase PV systems expands rapidly [1]. Instead of DC/AC power-conversion structures employing transformers for providing galvanic isolation, transformerless inverters are most frequently used to interface the energy produced by the PV source to the electrical grid in such PV installations, due to their lower cost, lower weight and higher efficiency [2-7].

According to the block diagram illustrated in Fig. 1, a grid-connected transformerless PV inverter is synthesized by combining a power section with an output filter. The power

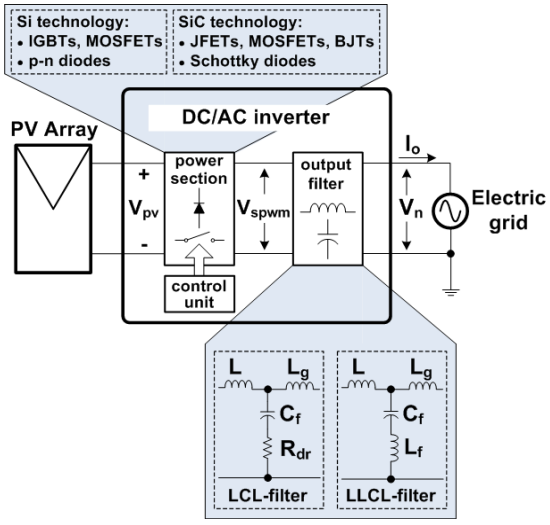

Fig. 1. A block diagram of a transformerless single-phase PV inverter interconnected with the electric grid and alternative power-semiconductors manufacturing technologies and output-filter topologies, which may be adopted in order to build the PV inverter.

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section is comprised of power semiconductor devices, which are controlled by a microelectronic control unit. Alternative power-section topologies, power-semiconductors manufacturing technologies, which are based on either Si- or SiC-based materials, and output-filter structures are currently available and may be adopted by the designer in order to build the PV inverter, as analyzed next.

Multiple transformerless power-section topologies, with different operational characteristics, have been proposed in the past. Among them, the H5 [8] and Conergy-Neutral Point Clamped (Conergy-NPC) [9] structures (Fig. 2) have been incorporated into commercially available PV inverters, since they have the advantages of low leakage-ground-current combined with a high efficiency [10-12].

Typically, IGBT-type power-switches and diodes based on Silicon (Si) are used to build the power section of the PV inverters shown in Figs. 1 and 2 [11]. However, the Silicon Carbide (SiC) technology has emerged during the last few years as an alternative for the design of power semiconductors employed in such DC/AC inverters [13-15]. Due to the lower switching energy demands of SiC transistors, the PV inverter switching frequency can be increased by a factor of 3-9, thus aiming to reduce the size and cost of the passive components in the output filter, as well as to increase the efficiency of the PV inverter [16-19]. Additionally, using SiC-type power semiconductors, more flexibility is obtained in terms of implementation of the power-converter cooling subsystem, due to their capability to operate at a higher temperature than Si-type devices [20-23].

The SiC JFETs and SiC Schottky diodes are considered more mature SiC technology for incorporation in the power-section of the PV inverters in Figs. 1 and 2 [24]. SiC JFETs are available commercially, which are capable to operate reliably in high temperature and high switching-speed applications [25] and SiC MOSFETs are developed with power handling capability similar to that of Si-based IGBTs [26]. An analysis of the power losses exhibited by a three-phase inverter consisting of SiC MOSFETs with a 400 kHz switching frequency is presented in [27], while the design of a 200 kHz single-phase inverter consisting of Si-type MOSFETs and SiC free-wheeling diodes is analyzed in [28], showing the technical feasibility of highly increasing the switching frequency compared to the conventional PV inverters. The design of a 40 kVA three-phase, full-bridge inverter with 10 parallel-connected SiC JFETs in each switch position is described in [29]. The resulting efficiency of the inverter at rated power exceeds 99.5 %. A half-bridge resonant inverter for induction heating applications, which is built using commercially available SiC JFETs, is presented in [30]. Experimental results are presented for a 446 kHz switching frequency of the inverter. The design of a gate drive circuit for assisting the commutation of SiC-JFETs in bridge circuits with high switching speed is analyzed in [31]. An appropriate model, which enables the optimal design of filters for the reduction of conducted electromagnetic interference in DC/AC inverters with SiC JFETs is presented in [32].

The switches of the PV inverter power section (Fig. 1) are typically controlled according to modulation schemes such as

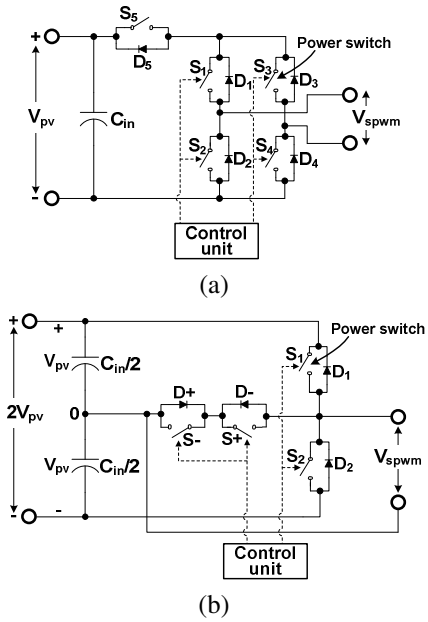

Fig. 2. The single-phase transformerless PV inverter topologies under study: (a) H5 and (b) Conergy-NPC.

the Sinusoidal Pulse Width Modulation (SPWM), the Space Vector Pulse Width Modulation (SVPWM) etc. In this case, the current produced by the power section contains multiple, high-frequency harmonics. Thus, a low-pass filter is connected at the output of the PV inverter power stage in order to reduce the amplitude of the current harmonics, which are injected into the electric grid, to an acceptable level [33]. Compared to the L-type filters, the LCL-filter structures are capable to fulfill the requirements set by grid-interconnection standards (e.g. IEEE 1542), in terms of the output current harmonic distortion, with significantly smaller size and cost and, simultaneously, they enhance the dynamic performance of the PV inverter, although their design-process is more challenging for the designer [34]. However, a high-order LLCL-type filter has also been introduced in [35, 36], targeting at an even better attenuation of the switching frequency current-ripple compared to the LCL-filter, thus leading to a further reduction of the filter size.

The PV inverters are typically designed without considering the impact of the continuously variable power generation of the PV array during the operational lifetime of the PV installation (mission profile), targeting to maximize the PV inverter maximum efficiency and/or the "European Efficiency", by iteratively evaluating power-loss and harmonic-current calculation models [3, 10, 11, 37, 38]. As an example, the LCL-filter employed in a grid-interactive voltage source inverter is designed in [39] by performing a sensitivity analysis in order to derive the values of the switching frequency and total filter inductance which minimize the total power loss of the filter. However, this design approach does not consider the impact of the switching frequency, the continuously varying output voltage/power of the PV power source and the LCL-filter component values, on the power loss of the power section.

In this paper, the design optimization methodology initially introduced in [37, 38] for PV inverters employing exclusively

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Si-type power semiconductors, is further advanced in order to accommodate the optimal design of H5 and Conergy-NPC transformerless PV inverters, which are based on the SiC technology. The proposed approach is based on the application of: (i) conventional power-electronic-circuit mathematical modeling techniques for calculating the power losses and manufacturing cost of the PV inverters and (ii) an optimization technique for deriving the optimal output-filter structure (either LCL- or LLCL-type) and switching frequency of the SiC-based power semiconductors, by investigating the simultaneous impacts of the mission profile (which is dictated by the meteorological conditions of the installation site), operational characteristics of the power semiconductors, power-section topology (i.e. H5 or Conergy-NPC) and output-filter structure, combined with a trade-off between the PV-inverter manufacturing cost and the power losses affecting the corresponding energy production. As demonstrated in the design results, this mixture of converter mathematical modelling and optimization processes offers to the proposed design technique the capability of deriving optimized configurations of the SiC-based transformerless H5 and Conergy-NPC PV inverters with superior performance compared to the corresponding PV inverters designed using the conventional approaches. Furthermore, the Levelized Cost Of the Electricity generated (LCOE) metric is typically used to evaluate the economic viability of grid-connected PV systems [40], since minimizing the cost of energy sold to the electric grid enables to maximize the net economic profit gained by the corresponding investment. Simultaneously, due to the variability of solar irradiation and ambient temperature conditions during the year, a PV inverter does not operate at a relatively constant operating point, as happens in applications such as uninterruptible power supplies, motor drives etc., but its input/output power levels change continuously, following the corresponding variation of meteorological conditions which prevail at the PV system installation site. Additionally, maximizing the PV inverter efficiency does not guarantee that the resulting configuration is economically attractive. Considering the above characteristics of PV systems, the LCOE metric has been employed in this work as the objective function of the PV inverter design optimization process, since it enables to derive the most economically attractive PV inverter configuration in terms of the cost of the total amount of energy generated by the PV system during the year. The design results presented in the paper verify that, compared to the non-optimized PV inverters, the inverters which have been optimally designed using the proposed methodology produce more total energy during the year and comprise components of lower cost.

This paper is organized as follows: the proposed design methodology is presented in Section II; the modeling of power losses and passive output-filters in H5 and Conergy-NPC transformerless PV inverters comprising SiC power devices are described in Sections III and IV, respectively; the design optimization results are analyzed in Section V and, finally, conclusions are discussed.

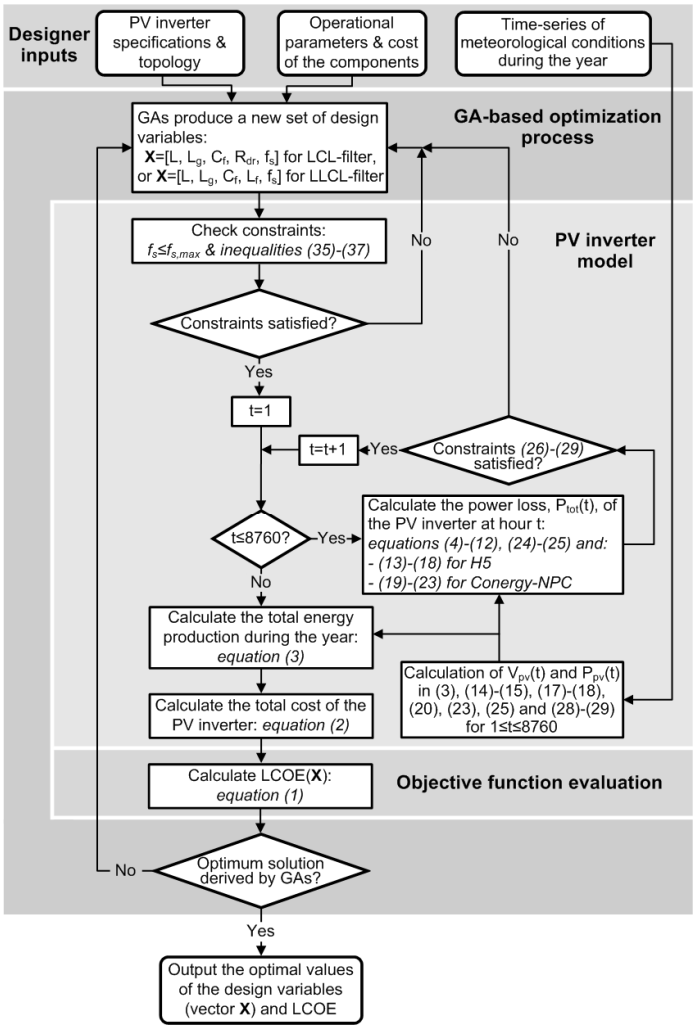

Fig. 3. A flow-chart of the proposed design procedure for optimizing SiC-based PV inverters.

II. The Proposed Design Optimization Methodology

The proposed design methodology enables to derive the optimal switching frequency of SiC-type power devices and optimize the configuration of the output filter (either LCL- or LLCL-type). A flow-chart illustrating the stages of the proposed design process, is depicted in Fig. 3. Initially, the designer of the PV inverter defines the following parameters:

- PV inverter specifications (e.g. power rating, nominal voltage/frequency of the electric grid etc.),
- power-section topology (i.e. H5 or Conergy-NPC) and output-filter structure (i.e. LCL- or LLCL-type),
- cost and operational characteristics of the SiC-type power semiconductors and filter components used to build the PV inverter (i.e. JFETs, inductors etc.), which are available by their manufacturer and
- time-series of the hourly-average solar irradiation and ambient temperature conditions, which prevail during the year at the installation site of the PV system.

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Then, an optimization process based on Genetic Algorithms (GAs) is employed in order to derive the optimal (i.e. minimum) value of the PV inverter Levelized Cost Of the Electricity generated, $LCOE$ (€/Wh), which comprises the objective-function of the proposed optimization process and is defined as [41]:

$$\underset{\mathbf{X}}{\text{minimize}}\left\{LCOE(\boldsymbol{X})\right\} = \underset{\mathbf{X}}{\text{minimize}}\left\{\frac{C_t(\boldsymbol{X})}{E_i(\boldsymbol{X})}\right\} \quad (1)$$

subject to : *design specifications & constraints are met*

where C_t (€) is the total manufacturing cost of the PV inverter, E_i (Wh) is the total energy injected into the electric grid by the PV inverter during a year and $\boldsymbol{X}$ is the vector of the design variables of the optimization process (i.e. $\boldsymbol{X}$ =[L, L_g, C_f, R_{dr}, f_s] for an LCL-type filter and $\boldsymbol{X}$ =[L, L_g, C_f, L_f, f_s] for an LLCL-type output filter in Fig. 1).

The values of C_t and E_i in (1) are calculated using a mathematical model of the SiC-based PV inverter, which is presented in the following. In the proposed design method, GAs are used to derive the optimal values of the PV inverter switching frequency, f_s (Hz) and output filter components, comprising vector $\boldsymbol{X}$ in (1), since they are capable to successfully solve complex optimization problems. During the GA-based optimization process, multiple alternative sets of values of the decision variables (i.e. vector $\boldsymbol{X}$) are produced and the corresponding values of $LCOE$ are calculated using (1). Among them, the overall optimum solution is the vector $\boldsymbol{X}$ which: (i) exhibits the minimum $LCOE$ and (ii) satisfies the constraints of the optimization problem, which are described in the following. This process is performed for each type of power-section topology (i.e. H5 or Conergy-NPC) and output filter (either LCL-, or LLCL-type) specified by the PV inverter designer.

Depending on the type of filter employed in the H5 and Conergy-NPC PV inverter, the value of the total construction cost, C_t in (1), is calculated as the sum of the prices of the individual components comprising each PV inverter structure as follows:

$$C_t(\boldsymbol{X}) = c_m + c_{hs} + n_s c_s + n_d c_d + c_I\left(L + L_g\right) + c_{L_f} L_f + \\ + c_c C_f + c_r R_{dr} \cdot SF \cdot P_{d,\max} \quad (2)$$

where c_m (€) is the manufacturing cost of the PV inverter without including the cost of the heat sink, power semiconductors and filter components, c_{hs} (€) is the cost of the heat sink, n_s, n_d, is the number of power switches and diodes, respectively, c_s, c_d (€) is the cost of each power switch and diode, respectively, c_I, c_{L_f} [€/H] is the cost per unit inductance of the filter inductors [L, L_g] and L_f, respectively, c_c (€/F) is the filter capacitor cost per unit capacitance, c_r [€/(Ω·W)] is the LCL-filter damping resistor cost per unit resistance and per unit power, SF (%) is the over-sizing factor of the LCL-filter damping resistor and $P_{d,\max}$ (W) is the maximum power dissipated on the LCL-filter damping resistor during the year.

For LCL-type filters it hold that $L_f = 0$ in (2), while in the case that an LLCL-filter is employed in the PV inverter output stage then $R_{dr} = 0$. The values of c_m, c_{hs}, c_s, c_d, c_I, c_{L_f}, c_c and c_r are obtained by the designer from the prices of the corresponding components, which are offered in the market and they are input in the proposed design process as shown in the flow-chart of Fig. 3.

The total energy injected into the electrical grid by the PV inverter during the year, $E_i(\boldsymbol{X})$ in (1), is calculated using a power-balance equation for each hour t of the year ($1 \le t \le 8760$), as follows:

$$E_i(\boldsymbol{X}) = \sum_{t=1}^{8760} P_o(t) \cdot \Delta t = \sum_{t=1}^{8760} \left[P_{pv}(t) - P_{tot}(t)\right] \cdot \Delta t \quad (3)$$

where P_o (W) is the power injected into the electrical grid, P_{pv} (W) is the Maximum Power Point (MPP) power produced by the PV array, which is connected at the DC input terminals of the PV inverter, P_{tot} (W) is the total power loss of the PV inverter and $\Delta t = 1$ hour is the simulation time-step.

In (3), the set of values of P_{pv}, as well as the corresponding values of the output voltage of the PV array V_{pv}, during the year constitute the PV inverter mission profile and they are calculated according to the models described in [42] using the time-series of the meteorological conditions during the year, which are provided by the PV inverter designer at the first step of the proposed process, as analyzed above. The total power loss of the PV inverter, P_{tot}, is calculated for each set of values comprising vector $\boldsymbol{X}$ in (1), by summing the power losses of the components comprising the power section, output filter and control unit:

$$P_{tot} = P_{cond} + P_{sw} + P_d + P_{L,c} + P_{L,r} + P_{cu} \quad (4)$$

where P_{cond}, P_{sw} (W) are the conduction and switching losses, respectively, of the SiC-type power semiconductors employed in the power section, P_d (W) is the power loss on the output-filter damping resistor (for an LLCL-filter $P_d = 0$), $P_{L,c}$, $P_{L,r}$ (W) are the core and winding losses, respectively, of the inductors incorporated in the LCL-type output filter and P_{cu} (W) is the total power consumption of the control unit, which is provided in the proposed optimization process by the PV inverter designer.

The values of P_d and $P_{L,c}$ are calculated as analyzed in [38]. The copper losses of the inductors, $P_{L,r}$ in (4), are calculated using the following equation:

$$P_{L,r} = I_r(t)^2 \cdot (R_{ac,L} + R_{ac,L_f}) + I_o(t)^2 \cdot r_L \cdot (L + L_g) + \\ + \frac{V_n^2 + [I_o(t) \cdot 2\pi f L_g]^2}{\left(2\pi f L_f - 1/C_f 2\pi f\right)^2 + (r_{L_f} \cdot L_f)^2} \cdot r_{L_f} \cdot L_f \quad (5)$$

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where $L_f = 0$ for an LCL-filter, $I_r(t)$ (A) is the RMS ripple current conducted by the inverter-side inductor (i.e. L in Fig. 1) at hour t of the year ($1 \le t \le 8760$), $I_o(t)$ (A) is the RMS value of the fundamental-frequency (i.e. 50 Hz) current, which is supplied by the PV inverter into the electric grid (Fig. 1), V_n (V) is the nominal RMS output voltage of the PV inverter, f (Hz) is the electric grid frequency, $R_{ac,L}$, R_{ac,L_f} (Ω) are the high-frequency resistances of the windings of inductors L and L_f, respectively and r_L, r_{L_f} (Ω/H) is the inductor winding low-frequency resistance per unit inductance of [L, L_g] and L_f, respectively.

The value of $R_{ac,L}$ in (5) is calculated considering the skin and proximity effects, as follows [43]:

$$R_{ac,L} = r_L L \frac{\gamma}{2}\left[\frac{ber(\gamma)\cdot bei'(\gamma) - bei(\gamma)\cdot ber'(\gamma)}{[ber'(\gamma)]^2 + [bei'(\gamma)]^2} - \lambda \frac{ber_2(\gamma)\cdot ber'(\gamma) + bei_2(\gamma)\cdot bei'(\gamma)}{[ber(\gamma)]^2 + [bei(\gamma)]^2}\right] \quad (6)$$

where γ and λ are constants, which depend on the switching frequency, f_s, as well as the construction characteristics of the inductor (e.g. conductor diameter, number of layers etc.) and ber, bei, ber_2 and bei_2 are the real and imaginary parts of the Bessel functions.

The same approach is also applied in order to calculate the value of R_{ac,L_f} in (5). The values of V_n, f, r_L, r_{L_f}, γ, λ in (5)-(6) are input in the proposed design process by the PV inverter designer. The total conduction and switching losses, P_{cond} and P_{sw} in (4), are calculated using the power-loss models for SiC-based H5 and Conergy-NPC PV inverters, which are presented in the next paragraph.

III. Power Loss Modeling of SiC-based H5 and Conergy-NPC PV Inverters

The proposed methodology is focused on H5 and Conergy-NPC transformerless PV inverters, which consist of SiC-based JFET power switches and Schottky diodes. The on-state voltages of these power devices are calculated using the following equations [19]:

$$V_s = I_S R_{s,on} \quad (7)$$

$$V_d = V_{d,on} + I_D R_{d,on} \quad (8)$$

where V_s, V_d (V) is the on-state voltage drop across the SiC JFET power switch and Schottky diode, respectively, I_S, I_D (A) is the corresponding conduction current, $V_{d,on}$ (V) is the on-state voltage drop on the Schottky diode when $I_D = 0$ and $R_{s,on}$, $R_{d,on}$ (Ω) is the on-state resistance of the power switch and diode, respectively.

The on-state resistances of SiC-based power JFETs and Schottky diodes depend on the junction temperature of the power semiconductor, T_j (°C) [19, 24]:

$$R_{pd,on} = c_1 \cdot T_j^2 + c_2 \cdot T_j + c_3 \quad (9)$$

where $R_{pd,on} = R_{s,on}$ or $R_{pd,on} = R_{d,on}$ for SiC-type JFETs and Schottky diodes in (7) and (8), respectively and c_1, c_2, c_3 are constants derived according to the corresponding information provided in the device datasheet.

The average and RMS values of the conduction current of each power switch or diode, I_{avg} and I_{rms} (A), are calculated as follows:

$$I_{avg} = \frac{1}{2\pi}\int_0^{2\pi} \sqrt{2}\cdot I_o(t)\cdot \sin(\phi - \theta)\cdot f(\phi, m_a)\cdot d\phi \quad (10)$$

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (\sqrt{2}\cdot I_o(t)\cdot \sin(\phi - \theta))^2 \cdot f(\phi, m_a)\cdot d\phi} \quad (11)$$

where $f(\phi, m_a)$ is the modulation function of the corresponding power semiconductor [37], m_a is the modulation index of the SPWM voltage produced by the power section of the PV inverter at hour t (i.e. V_{spwm} in Figs. 1 and 2) [38] and θ (rad) is the phase angle between the PV inverter output current and the fundamental-frequency component of V_{spwm}.

The value of the modulation function $f(\phi, m_a)$ is set equal to zero for the time intervals that the corresponding SiC-type JFET or Schottky diode does not conduct current. The phase angle θ in (10) and (11) is calculated as follows:

$$\cos\theta = V_n \Big/ \sqrt{V_n^2 + \left[I_o(t) 2\pi f \left(L + L_g\right)\right]^2} \quad (12)$$

The values of the total conduction and switching losses, P_{cond} and P_{sw} in (4), are given by the sum of the corresponding power losses developed in each of the SiC-type power switches and diodes of the H5 and Conergy-NPC PV inverters, which are subject to the proposed optimization procedure, as analyzed next.

A. H5 PV inverter

The total conduction loss of the H5 PV inverter at hour t of the year ($1 \le t \le 8760$), $P_{cond}(t)$ (W), is equal to the sum of the conduction losses of the SiC-type JFETs and Schottky diodes comprising its power section and it is calculated using (7)-(12), according to the following equation:

$$\begin{aligned} P_{cond}(t) = {} & 2\cdot I_{S1,rms}^2 R_{s,on} + 2\cdot I_{S4,rms}^2 R_{s,on} + I_{S5,rms}^2 R_{s,on} + \\ & + 2\cdot (V_{d,on} I_{D1,avg} + I_{D1,rms}^2 R_{d,on}) + V_{d,on} I_{D5,avg} + \\ & + 2\cdot (V_{d,on} I_{D4,avg} + I_{D4,rms}^2 R_{d,on}) + I_{D5,rms}^2 R_{d,on} \end{aligned} \quad (13)$$

where $I_{i,avg}$, $I_{i,rms}$ (A) are the average and RMS values, respectively, of the current conducted by the i-th power device (see Fig. 2).

The values of $I_{D1,avg}$, $I_{D4,avg}$, $I_{D5,avg}$, $I_{D1,rms}$, $I_{D4,rms}$, $I_{D5,rms}$, $I_{S1,rms}$, $I_{S4,rms}$ and $I_{S5,rms}$ in (13) are calculated by applying the modulation functions for the H5 PV inverter in (10) and (11), respectively, as presented in [37].

The switching loss of each SiC-type JFET employed in the

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H5 PV inverter, P_J (W), is calculated using the following equation [19]:

$$P_J = \left(\frac{V_{pv}(t)}{V_{ref}}\right)^{\frac{3}{2}} \cdot f_s \cdot \frac{1}{2\pi} \cdot \int_0^{2\pi} E(\lambda) d\lambda \quad (14)$$

where $V_{pv}(t)$ (V) is the output voltage of the PV array at hour t of the year ($1 \le t \le 8760$), V_{ref} (V) is the reference (test) voltage and $E(\cdot)$ is the switching energy consumption, which is calculated as a third-order polynomial function of the current conducted by the SiC-type JFET [44].

The H5 PV inverter topology operates symmetrically during a period of the fundamental-frequency component of the SPWM signal V_{spwm} in Figs. 1 and 2. Thus, the total switching energy of power switches S_1, S_4 and S_5 during the time interval [θ, π+θ] is equal to the total switching energy of S_2, S_3 and S_5 at [π+θ, 2π+θ]. Applying (14), it results in that the total switching power loss during [0, 2π] of all JFETs in the H5 PV inverter at hour t of the year, $P_{sw,s}(t)$ (W), is given by:

$$P_{sw,s}(t) = 2 \cdot f_s \cdot \left(\frac{V_{pv}(t)}{V_t}\right)^{\frac{3}{2}} \cdot E_{sw1} \quad (15)$$

where the switching energy E_{sw1} (Joule) is calculated using the following equation:

$$\begin{aligned} E_{sw1} = {} & \alpha_1 \cdot I_o(t)^3 \cdot \left(2 + \frac{3\cos\theta}{4} - \frac{\cos 3\theta}{12}\right) + \\ & + \alpha_2 \cdot I_o(t)^2 \cdot \left(\pi - \frac{\theta}{2} + \frac{\sin 2\theta}{4}\right) + \\ & + \alpha_3 \cdot I_o(t) \cdot (3 + \cos\theta) \end{aligned} \quad (16)$$

and the values of coefficients α_1 - α_3 are derived as described in [44] using the switching-energy/conduction-current characteristic, which is provided in the datasheet of the considered SiC device.

The switching power loss of each SiC-type Schottky diode of the H5 PV inverter, P_D (W), is calculated according to [19], using the following equation:

$$P_D = f_s \cdot \frac{V_{pv}(t)}{2S} \cdot \sqrt{\frac{V_{pv}(t)}{V_t}} \cdot I_R \cdot t_{rr} \cdot \frac{S^2}{S+1} \quad (17)$$

where S is the diode snappiness factor, I_R (A) is the peak reverse-recovery current and t_{rr} (sec) is the reverse-recovery time, respectively.

The values of S, I_R and t_{rr} are derived from the datasheet of the Schottky diode employed in the H5 inverter power section. Due to symmetrical operation, the total switching power loss of D_2, D_3 and D_5 during [θ, π+θ] is equal to that developed in D_1, D_4 and D_5 during the time interval [π+θ, 2π+θ]. Thus, the total switching losses of all Schottky diodes included in the H5 PV inverter at hour t of the year, $P_{sw,d}(t)$ (W), are calculated using (17), according to the following equation:

$$P_{sw,d}(t) = \left(1 + \frac{\theta}{\pi}\right) \cdot f_s \cdot \frac{V_{pv}(t)}{2S} \cdot \sqrt{\frac{V_{pv}(t)}{V_t}} \cdot I_R \cdot t_{rr} \cdot \frac{S^2}{S+1} \quad (18)$$

B. Conergy-NPC PV inverter

Similarly to the approach applied for the H5 PV inverter, the total conduction loss at hour t of the year ($1 \le t \le 8760$), $P_{cond}(t)$ (W), of the SiC-type power semiconductors comprising the Conergy-NPC PV inverter are calculated using (7)-(12), by summing the conduction losses developed at the individual SiC JFETs and Schottky diodes, as follows:

$$\begin{aligned} P_{cond}(t) = {} & 2 \cdot I_{S1,rms}^2 R_{s,on} + 2 \cdot (V_{d,on} I_{D1,avg} + I_{D1,rms}^2 R_{d,on}) + \\ & + 2 \cdot I_{S+,rms}^2 R_{s,on} + 2 \cdot (V_{d,on} I_{D+,avg} + I_{D+,rms}^2 R_{d,on}) \end{aligned} \quad (19)$$

Considering the symmetrical operation of the Conergy-NPC PV inverter, it is concluded that the switching energy of $S+$ and S_1 at [θ, π+θ] is equal to that of $S-$ and S_2 during [π+θ, 2π+θ]. Then, the total switching loss during [0, 2π] of all SiC-type JFET power switches incorporated in the Conergy-NPC inverter, $P_{sw,s}(t)$ (W), is derived using (14), as follows:

$$P_{sw,s}(t) = 2 \cdot f_s \cdot \left(\frac{V_{pv}(t)}{V_t}\right)^{\frac{3}{2}} \cdot \left(E_{sw2} + \frac{E_{sw3}}{2}\right) \quad (20)$$

where the switching energies E_{sw2} and E_{sw3} (Joule) are given by the following equations:

$$\begin{aligned} E_{sw2} = {} & \alpha_1 \cdot I_o(t)^3 \cdot \left(\frac{2}{3} + \frac{3\cos\theta}{4} - \frac{\cos 3\theta}{12}\right) + \\ & + \alpha_2 \cdot I_o(t)^2 \cdot \left(\frac{\pi - \theta}{2} + \frac{\sin 2\theta}{4}\right) + \\ & + \alpha_3 \cdot I_o(t) \cdot (1 + \cos\theta) \end{aligned} \quad (21)$$

$$E_{sw3} = \alpha_4 \cdot I_o(t)^3 + \alpha_5 \cdot I_o(t)^2 + \alpha_6 \cdot I_o(t) \quad (22)$$

and the values of α_4 - α_6 are derived according to [44], as described above.

Also, due to symmetrical operation, the switching losses of the SiC-type Schottky diodes $D+$ and D_2 during [θ, π+θ] are equal to the switching losses of $D-$ and D_1 at [π+θ, 2π+θ]. Using (17), it results in that the total switching loss of all Schottky diodes included in the power section of the Conergy-NPC inverter, $P_{sw,d}(t)$ (W), is given by:

$$P_{sw,d}(t) = \left(1 + \frac{\theta}{\pi}\right) \cdot f_s \cdot \frac{V_{pv}(t)}{2S} \cdot \sqrt{\frac{V_{pv}(t)}{V_t}} \cdot I_R \cdot t_{rr} \cdot \frac{S^2}{S+1} \quad (23)$$

In the proposed optimization methodology it is assumed that the power switches and diodes of both the H5 and Conergy-NPC inverters are mounted on a common heat sink. Thus, the junction temperature of each SiC-type power semiconductor incorporated to the power section of the H5 and Conergy-NPC PV inverters at each hour t of the year ($1 \le t \le 8760$), $T_{j,i}(t)$ ($^{\circ}$C), is given by the following equation:

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$$T_{j,i}(t) = T_A(t) + \theta_{jc} \cdot P_{l,i}(t) + \theta_{ca} \cdot \sum_{k=1}^{n} P_{l,k}(t) \quad (24)$$

where $T_A(t)$ ($^{\circ}$C) is the ambient temperature of the PV inverter at hour t, θ_{jc} ($^{\circ}$C/W) is the junction-to-case thermal resistance of the i-th power semiconductor, θ_{ca} ($^{\circ}$C/W) is the thermal resistance of the heat sink, n is the number of power semiconductors comprising the PV inverter power section ($n=10$ and $n=8$ for the H5 and Conergy-NPC topologies, respectively) and $P_{l,i}(t)$ (W) is the total conduction and switching power loss of the i-th power device at hour t ($1 \le i \le n$).

However, the total power loss of the H5 and Conergy-NPC PV inverters, as well as the junction temperature of the SiC-based semiconductors they comprise, given by (4) and (24), respectively, depend on both the output current, $I_o(t)$ and the junction temperature of the SiC-based power semiconductors, $T_{j,i}(t)$, at hour t of the year. Thus, in the proposed methodology, the values of $I_o(t)$ and $T_{j,i}(t)$ are calculated for each hour t of the year ($1 \le t \le 8760$), by solving numerically the system of equations comprised of (24) for all power semiconductors of the PV inverter and the following power-balance equation:

$$P_{pv}(t) = P_{tot}(t) + V_n \cdot I_o(t) \quad (25)$$

Additionally, for each hour t of the year ($1 \le t \le 8760$), the junction temperature of the SiC-type power devices, given by (24), is constrained during the execution of the proposed design process as follows:

$$T_{j,i}(t) \le T_{j,max} \quad (26)$$

where $T_{j,max}$ ($^{\circ}$C) is the junction-temperature limit for safe operation, which is specified by the manufacturer of the SiC-type power device, or by the designer in order to achieve a specified failure rate.

During the execution of the proposed design process, (7)-(9), (13), (15)-(24) and (26), respectively, are evaluated according to the flow-chart shown in Fig. 3 using the values of $V_{d,on}$, c_1-c_3, α_1-α_6, S, I_R, t_{rr}, θ_{jc}, θ_{ca} and $T_{j,max}$ which are provided by the PV inverter designer.

IV. Modeling of Passive Filters

In the proposed methodology, it is assumed that the H5 and Conergy-NPC PV inverters are controlled such that a unipolar SPWM signal is produced at the output of the power section (i.e. V_{spwm} in Figs. 1 and 2). Also, as illustrated in Fig. 1, the LCL-filter employs a damping resistor, R_{dr}, in series with the filter capacitor [34], while in the LLCL-type filter an inductor, L_f, is used instead of R_{dr} [35]. Both the LCL- and LLCL-type filters are designed such that at each hour t of the year ($1 \le t \le 8760$) the ripple factor of the current at the inverter side, RF_{sw} (%), is less than the maximum limit, which is defined by the PV inverter designer, $RF_{sw,max}$ (%):

$$RF_{sw} = \frac{I_r(t) \cdot V_n}{P_n} \le RF_{sw,max} \quad (27)$$

where P_n (W) is the nominal power rating of the PV inverter. Furthermore, at each hour t of the year ($1 \le t \le 8760$), the PV inverter output current harmonics at both the switching frequency and at the double of the switching frequency are constrained to be less than the maximum permissible limit, $RF_{\max}$ (%), which is specified by the PV inverter designer, as follows [35]:

$$\frac{2V_{pv}(t) \cdot V_n \cdot |G(j\omega_s)| \cdot \max\left(|J_1(\pi m_a)|, |J_3(\pi m_a)|\right)}{\sqrt{2}\pi P_n} \le RF_{\max} \quad (28)$$

$$\max\left(|J_1(2\pi m_a)|, |J_3(2\pi m_a)|, |J_5(2\pi m_a)|\right) \cdot \frac{V_{pv}(t) \cdot V_n \cdot |G(j2\omega_s)|}{\sqrt{2}\pi P_n} \le RF_{\max} \quad (29)$$

where:

$$G(s) = \frac{L_{ripple} C_f s^2 + 1}{\left(LL_g C_f + \left(L + L_g\right) L_{ripple} C_f\right) s^3 + \left(L + L_g\right) s} \quad (30)$$

and $L_{ripple} = 0$ for an LCL-filter and J_1, J_3 and J_5 are the integrals of the Bessel function, defined as $J_n(x) = (1/\pi)\int_0^{\pi} \cos(n\lambda - x\sin\lambda) d\lambda$.

In order also to take into account the deviation of L_{ripple} from its nominal value in real applications of the LLCL-filter, inequalities (28) and (29) are required to be valid for $L_{ripple} = 0.8L_f$, $L_{ripple} = L_f$ and $L_{ripple} = 1.2L_f$, respectively. The values of P_n, $RF_{sw,max}$, $RF_{\max}$ in (27)-(29) are input in the proposed design process by the PV inverter designer.

The value of the LCL-filter damping resistor is calculated as a function of the filter capacitor, C_f, and the resonance frequency, f_{res}:

$$R_{dr} = \frac{1}{2\pi C_f f_{res}} \quad (31)$$

where:

$$f_{res} = \frac{1}{2\pi} \cdot \sqrt{(L + L_g) / L_g C_f L} \quad (32)$$

The resonant frequency of the LLCL-filter is given by:

$$f_{res} = \frac{1}{2\pi} \cdot \frac{1}{\sqrt{(L_g \cdot L / (L + L_g) + L_f) \cdot C_f}} \quad (33)$$

For LLCL-type filters, the value of L_f is calculated such that the $L_f - C_f$ branch resonates at the switching frequency:

$$L_f = \frac{1}{(2\pi f_s)^2 C_f} \quad (34)$$

in order to filter out this harmonic for the grid side and lower the overall Total Harmonic Distortion (THD) of the output current.

Furthermore, the values of the components comprising the

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TABLE I
THE OPTIMAL VALUES OF THE DESIGN VARIABLES AND *LCOE* FOR H5 AND CONERGY-NPC PV INVERTERS WITH AN LCL-TYPE OUTPUT FILTER, FOR VARIOUS INSTALLATION SITES IN EUROPE.

Installation site and power section topology		L (mH)	L_g (μH)	C_f (μF)	R_{dr} (Ω)	f_s (kHz)	$LCOE_{opt}$ (€/MWh)	$LCOE_{Si}$ (€/MWh)	$LCOE_{n\text{-}o}$ (€/MWh)
Athens	**H5**	0.165	5.599	3.329	1.276	170.60	252.99	231.62	284.48
	Conergy-NPC	0.396	8.583	1.024	2.865	212.10	244.95	228.57	276.81
Murcia	**H5**	0.176	4.502	3.309	1.152	179.15	224.22	204.74	250.55
	Conergy-NPC	0.352	2.356	1.516	1.243	236.50	216.93	201.89	243.66
Freiburg	**H5**	0.158	7.537	3.316	1.473	174.85	362.91	337.55	421.15
	Conergy-NPC	0.412	6.109	1.007	2.446	209.65	352.86	333.09	409.81
Oslo	**H5**	0.151	4.040	2.733	1.199	216.75	367.96	342.98	425.20
	Conergy-NPC	0.411	27.135	1.273	4.472	218.20	358.07	338.70	413.83

PV inverter filter (either LCL- or LLCL-type) are additionally limited during the execution of the proposed optimization process according to the following constraints [34, 35]:

- in order to avoid excessive AC voltage drop during the operation of the PV inverter (and thereby high DC-link voltage), the sum of L and L_g is limited to be less than 0.1 pu:
$$L + L_g \le 0.1 \cdot L_b \tag{35}$$
where $L_b = V_n^2 / (P_n 2\pi f)$ is the base inductance.
- the value of the filter capacitor, C_f, must be less than 0.05 pu in order to limit the reactive power flow in the output-filter capacitor:
$$C_f \le 0.05 \cdot C_b \tag{36}$$
where $C_b = P_n / (V_n^2 2\pi f)$ is the base capacitance.
- to avoid resonance problems, the value of f_{res} for both filter types is set as follows:
$$10 \cdot f \le f_{res} \le \frac{f_s}{2} \tag{37}$$

where f (Hz) is the nominal frequency of the electric grid voltage (e.g. 50 Hz).
By increasing the switching frequency to 100-300 kHz, such constraints are easier to fulfill.

V. DESIGN OPTIMIZATION RESULTS

Targeting to demonstrate the capabilities of the proposed optimization methodology and evaluate the performance of optimized SiC-based PV inverters in various installation sites, the design optimization of single-phase transformerless H5 and Conergy-NPC PV inverters with a 2 kW rated power capacity, which are interconnected with a 220 V / 50 Hz electric grid with unity power factor, has been performed as analyzed in the previous sections. A design tool has been developed for that purpose in the form of a MATLAB software program, which implements the methodology presented in § II-IV according to the design stages depicted in the flow-chart of Fig. 3. The SiC-based PV inverters have been optimized for operation in Murcia (Spain), Athens (Greece), Freiburg (Germany) and Oslo (Norway), respectively. Also, the operational characteristics of commercially-available 1200 V SiC-type JFETs and Schottky diodes with a maximum permissible switching frequency $f_{s,\max} = 300\,\text{kHz} \ge f_s$ have been provided as inputs in the proposed design optimization process. The values of $RF_{sw,max}$ and RF_{max} have been set equal to 10 % and 0.3 %, respectively, such that the designed PV inverters conform to the requirements of the IEEE 519-1992 standard. Considering the low power-loss features of SiC devices, the system of equations which must be solved numerically for calculating the values of $I_o(t)$ and $T_{j,i}(t)$, as analyzed in § III, is substantially simplified by setting $\theta_{jc} = 0$ in (24) for all power devices of the PV inverter. Hence, the corresponding computational complexity is alleviated and the execution time of the optimization process is decreased significantly. Applying this approach resulted in a maximum error of less than 0.2 % in the calculated LCOE values.

The optimal values of the design variables L, L_g, C_f, R_{dr} and f_s, comprising vector $\boldsymbol{X}$ in (1) and the corresponding optimal values of the cost of electricity (i.e. $LCOE_{opt}$) for H5 and Conergy-NPC PV inverters with an LCL-type output filter, which have been separately optimized for each installation site in order to investigate the impact of mission profile, are presented in Table I. The resulting optimal values of the design variables L, L_g, C_f, R_{dr} and f_s are different for each power section topology (i.e. H5 or Conergy-NPC) and installation site. This is due to: (i) the different operational characteristics of each PV inverter topology, affecting the corresponding power losses and total cost of the PV inverter and (ii) the different time-series of yearly solar irradiation and ambient temperature prevailing in each site, which define the variation during the year of the output voltage and power of the PV array connected to the DC input terminals of the PV inverter (mission profile). Thus, different power losses are developed in the H5 and Conergy-NPC PV inverters in each installation site during the year, affecting both the total energy production and the resulting optimal values of the design variables which minimize

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the LCOE metric. The LCOE of the optimized SiC-based Conergy-NPC PV inverters is lower by 2.69-3.25 %, compared to that of the optimized inverters employing an H5 topology in their power section.

In order to compare their performance in terms of cost and energy production, non-optimized SiC-based H5 and Conergy-NPC PV inverters operating with $f_s = 15\,\text{kHz}$, as well as optimized H5 and Conergy-NPC PV inverters consisting of commercially available Si-type IGBTs and power diodes with $f_{s,\max} = 30\,\text{kHz}$ have also been designed for the same installation sites, such that, in both of these cases, the constraints (27)-(29) are also satisfied. The non-optimized SiC-based inverters have been designed according to the procedure described in [34], where, in contrast to the proposed design process, the values of L, L_g, C_f and R_{dr} are calculated without taking into account the cost and energy production performance of the PV inverter and also without exploring the entire search-space in order to derive the optimum combination of values of the output-filter components. The optimized Si-type inverters have been designed as analyzed in [37]. The values of $LCOE_{opt}$ in Table I are higher than those of optimized PV inverters comprised of Si-based power semiconductors ($LCOE_{Si}$ in Table I) by 5.72-9.51 %, due to the higher current market prices of SiC-type devices. The LCOE of the non-optimized SiC-based H5 and Conergy-NPC PV inverters ($LCOE_{n\text{-}o}$ in Table I) is higher than that of their optimized counterparts by 11.74-16.14 %, thus demonstrating the capability of the proposed design methodology to derive PV inverter configurations with improved performance in terms of LCOE. The optimal values of L, L_g, C_f and R_{dr} in the high-frequency SiC-based PV inverters, presented in Table I, are equal to 5.05-14.32 %, 2.86-22.12 %, 18.45-121.38 % and 22.35-146.67 %, respectively, of the corresponding values in the optimized Si-based inverters. Similarly, the optimal switching frequency of the SiC-based inverters, f_s, is 5.81-7.88 times higher than that of the optimized PV inverters employing Si-type devices. Thus, since the dimensions of the output-filter inductors are determined by their inductance, it is concluded that the exploitation of the high-frequency operating capability provided by the SiC power-semiconductor technology results in a substantial reduction of the weight and size of the output-filter inductors in the optimized PV inverter structures, which have been derived using the proposed design optimization method. The optimal values of C_f and R_{dr} are in some cases higher in the optimized SiC-type inverters than in the inverters built using Si-type devices, but due to the small weight and size of these components, the impact of such an increase on the overall size and weight of the PV inverter is negligible.

The total energy injected into the electric grid by the non-optimized and optimized Si- and SiC-based PV inverters in each installation site is illustrated in Fig. 4. Compared to the H5 and Conergy-NPC PV inverters, which have been optimally designed using the proposed method, the non-optimized SiC-based PV inverters produce less energy in the range of

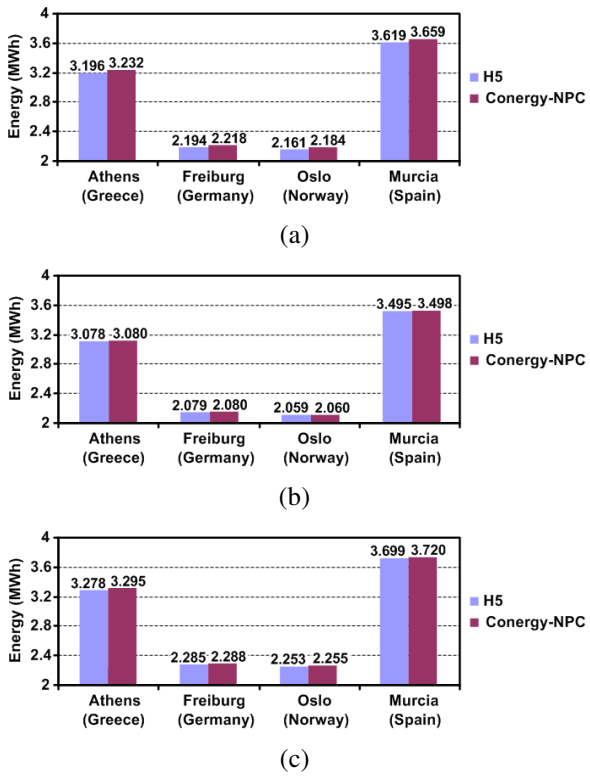

Fig. 4. The total energy injected into the electric grid by the H5 and Conergy-NPC PV inverters: (a) optimized Si-based, (b) non-optimized SiC-based and (c) optimized SiC-based.

5.52-9.09 %. The energy production of the optimized SiC-based PV inverters is higher by 1.67-4.26 % compared to that of the optimized H5 and Conergy-NPC inverters comprising Si-type devices. This is achieved due to the reduction of the filter-inductors size and the relatively low switching-loss of SiC-type power semiconductors, which are obtained when operating with a high switching frequency.

The total cost of the power-section and output-filter components employed in the non-optimized and optimized SiC- and Si-based H5 and Conergy-NPC PV inverters, in each installation site, is depicted in Fig. 5. The components cost of the non-optimized SiC-based PV inverters is higher than that of the optimized H5 and Conergy-NPC SiC-type structures by 38.89-47.06 %. Also, the components cost of the optimized SiC-based PV inverters is higher than that of the optimized PV inverters comprising Si-type power devices by 226.53-293.27 %, due to the higher market prices of SiC-based power semiconductors. The component cost of the optimized Si- and SiC-based Conergy-NPC PV inverters is lower by 4.07-5.67 % and 18.04-18.80 %, respectively, compared to the cost of their H5 counterparts, thus being operationally and economically more effective in the specific installation sites considered.

The cost of SiC-based power semiconductors should be reduced to 38.6-52.3 % of their current market price in order to obtain equal LCOE with the PV inverters employing Si-based semiconductors. For equally priced Si- and SiC-type components, the optimized, high-frequency SiC-based PV

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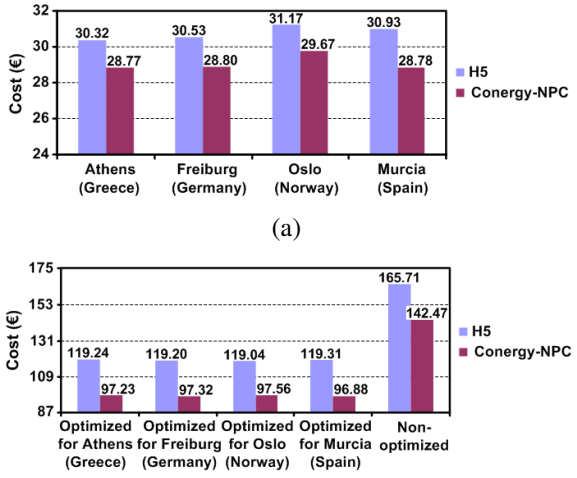

Fig. 5. The total cost of the power-section and output-filter components in the H5 and Conergy-NPC PV inverters: (a) optimized Si-based and (b) optimized and non-optimized SiC-based.

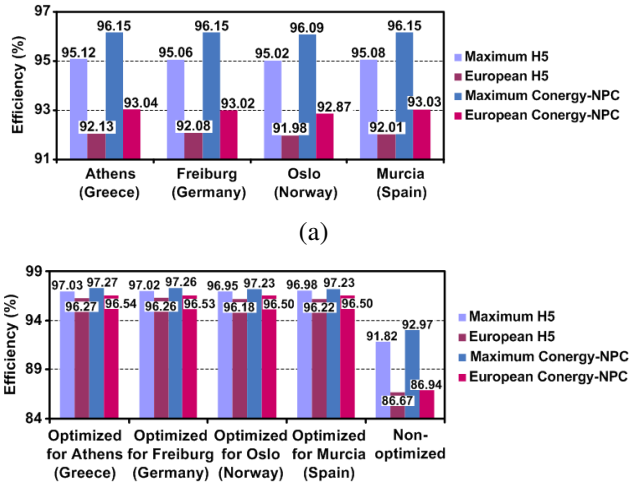

Fig. 6. The maximum efficiency and European efficiency of the H5 and Conergy-NPC PV inverters: (a) optimized Si-based and (b) optimized and non-optimized SiC-based.

inverters achieve lower LCOE by 4.19-6.69 %, higher energy production by 1.59-4.16 % and lower total manufacturing cost by 2.69-2.94 % compared to the optimized Si-based inverters.

As analyzed above, the optimal values of the design variables, comprising vector $\boldsymbol{X}$ in (1), are different for each installation site (Table I). However, in case that the H5 and Conergy-NPC SiC-based PV inverters which have been optimally designed for Oslo are also installed in Athens, Murcia and Freiburg, then the resulting values of LCOE are lower than those of the non-optimized inverter by 10.50-13.87 %. Also, the corresponding energy production is higher than that of the non-optimized inverter by 5.78-9.95 %. Thus, it is concluded that in order to comply with the uniform-construction requirements of massively-produced industrial PV inverter products, using the proposed design optimization methodology enables to derive a unique optimized PV inverter structure with superior performance, compared to its non-optimized counterpart, over wide geographical areas.

The maximum efficiency and European efficiency of the non-optimized and optimized SiC- and Si-based H5 and Conergy-NPC PV inverters in each installation site are depicted in Fig. 6. Since in the proposed design process the LCOE metric was minimized, optimized PV inverter structures were derived, which were capable to produce more total energy during the year [i.e. E_i in (1)] by featuring higher efficiency. Thus, the SiC-based PV inverters, which have been optimally designed using the proposed design technique, exhibit higher maximum efficiency and European efficiency by 4.58-5.67 % and 10.97-11.08 %, respectively, than their non-optimized counterparts. Also, the maximum efficiency and European efficiency of the optimized SiC-based H5 and Conergy-NPC PV inverters are higher than those of the optimized PV inverters based on Si technology by 1.12-2.06 % and 3.73-4.58 %, respectively.

In order to demonstrate the impact of the output-filter type on the design optimization results, the proposed methodology has also been applied for the case that an LLCL-type filter (see Fig. 1) is employed in H5 and Conergy-NPC PV inverters optimally designed for Murcia (Spain), which is the installation site exhibiting the highest solar irradiation potential. The resulting optimal values of the design variables L, L_g, C_f, L_f and f_s, comprising vector $\boldsymbol{X}$ in (1) and the corresponding optimal values of the cost of electricity (i.e. $LCOE_{opt}$), for all combinations of alternative power-semiconductor types and power-section topologies employed in the PV inverter, are presented in Table II. The optimal values of the design variables are different for each power-section topology and power-semiconductor manufacturing technology, respectively, due to the different operational characteristics of the PV inverter system in each of the alternative combinations examined. Non-optimized LCL- and LLCL-type filters have been designed by following the procedures described in [34] and [35], respectively, such that constraints (27)-(29) are also satisfied, for H5 and Conergy-NPC PV inverters operating with $f_s = 15$ kHz. Similarly to the case described above, the entire range of output-filter components values has also not been explored when designing these non-optimized inverters. The values of $LCOE_{opt}$ in Table II are lower than those of the non-optimized H5 and Conergy-NPC PV inverters, $LCOE_{n\text{-}o}$, by 6.54-10.40 %.

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TABLE II
THE OPTIMAL VALUES OF THE DESIGN VARIABLES AND *LCOE* FOR H5 AND CONERGY-NPC PV INVERTERS DESIGNED FOR INSTALLATION IN MURCIA (SPAIN), IN CASE THAT AN LLCL-TYPE OUTPUT FILTER IS USED.

Types of power semiconductors and power-section topology		L (mH)	L_g (μH)	C_f (μF)	L_f (μH)	f_s (kHz)	$LCOE_{opt}$ (€/MWh)	$LCOE_{n\text{-}o}$ (€/MWh)
H5	**Si**	2.992	26.07	1.94	16.77	27.90	204.54	219.81
	SiC	0.336	1.02	1.01	0.41	247.50	224.26	250.28
Conergy-NPC	**Si**	2.840	13.70	3.15	8.97	29.95	201.64	215.75
	SiC	0.411	1.01	1.01	0.61	202.30	217.08	242.14

The total cost and yearly energy production, C_t and E_i in (1)-(3), of the optimized PV inverter structures presented in Tables I and II for Murcia (Spain) for all combinations of power-section topology (H5 or Conergy-NPC), power-devices manufacturing technology (Si- or SiC-based) and output-filter type (LCL- or LLCL-type), are illustrated in Figs. 7(a) and (b), respectively. The upper limit of f_{res} in (37) has been extended up to $0.65 \cdot f_s$ in order to explore the performance of the PV inverters over a wider frequency range. The cost of the optimized SiC-based inverters is higher than that of the H5 and Conergy-NPC inverters employing Si-type power semiconductors by 9.22-12.10 %, due to the higher cost of SiC devices, but the SiC-based inverters inject more energy into the electric grid by 1.68-2.24 %. The energy production of the non-optimized H5 and Conergy-NPC PV inverters with an LLCL filter is lower than that of the corresponding optimized PV inverters by 2.65-5.40 % and their cost is higher by 3.26-5.58 %. In the cases under study, the cost and energy production of the optimized PV inverters employing LLCL- and LCL-type filters, respectively, differ by less than 0.1 %.

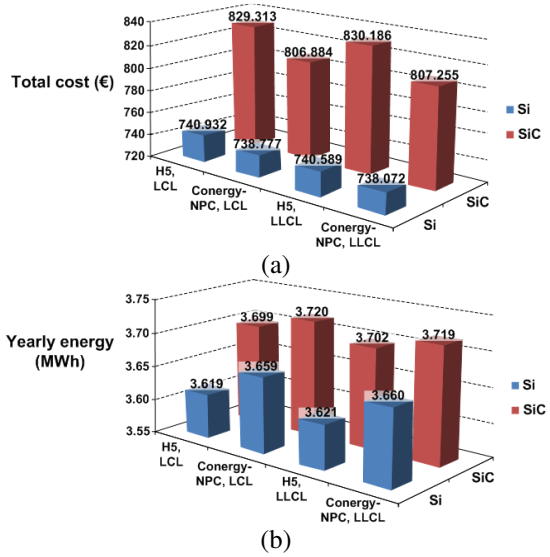

Fig. 7. The performance of optimized PV inverters for Murcia (Spain) for all combinations of power-section topology, power-devices manufacturing technology and output-filter type: (a) total cost and (b) yearly energy production.

VI. CONCLUSIONS

The transformerless DC/AC inverters are critical components in the rapidly growing market of grid-connected PV systems. Additionally, the application of SiC technology has emerged during the last years for the construction of power-semiconductor devices employed in energy conversion systems, with high operating temperature and frequency capabilities. Thus, multiple alternatives are currently available to designers in terms of the power-section topology, power-semiconductors manufacturing technology and configuration of the output filter, which may be adopted in order to synthesize transformerless PV inverter structures. In this paper, a new design technique has been presented for optimizing the switching frequency and structure of the output filter (either LCL- or LLCL-type) in transformerless H5 and Conergy-NPC PV inverters, which employ SiC-type power semiconductors. The proposed technique comprises an integrated design tool, which incorporates into the design process the simultaneous impact of the factors affecting the PV energy processing performance and the PV inverter cost.

The design results demonstrate that the optimized SiC-based H5 and Conergy-NPC transformerless PV inverters, which are derived using the proposed methodology, are more effective in terms of energy production than their non-optimized and Si-based counterparts. Also, they are capable to operate efficiently at higher switching frequencies, thus reducing the size, weight and cost of the PV inverter output filter. Finally, it has been shown that the reduction of the market price of SiC-type power semiconductors to the level of Si-based technology is the key factor in order to achieve the development of optimized SiC-based PV inverters with a lower cost of energy than the corresponding PV inverters employing Si technology, thus maximizing the economic profitability of the PV system.

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Stefanos Saridakis was born in Heraklion, Greece, in 1980. He received the B.Sc. degree in Electrical Engineering from the Technological Educational Institute of Crete (Heraklion, Greece) in 2004 and the Diploma in Electrical and Computer Engineering from the Democritus University of Thrace (Xanthi, Greece) in 2011. Currently, he is working towards the M.Sc. degree at the Department of Electronic and Computer Engineering of the Technical University of Crete (Chania, Greece). His research interests include power electronics for Renewable Energy Sources, electric machines and high-voltage direct-current power systems.

Eftichios Koutroulis (M'10) was born in Chania, Greece, in 1973. He received his B.Sc. and M.Sc. degrees in the School of Electronic and Computer Engineering of the Technical University of Crete (Chania, Greece) in 1996 and 1999, respectively. He received his Ph.D. degree in the School of Electronic and Computer Engineering of the Technical University of Crete in 2002 in the area of power electronics and Renewable Energy Sources (RES). He is currently an Assistant Professor at the School of Electronic and Computer Engineering of the Technical University of Crete. His research interests include power electronics (DC/AC inverters, DC/DC converters), the development of microelectronic energy management systems for RES and the design of photovoltaic and wind energy conversion systems.

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Frede Blaabjerg (S'86–M'88–SM'97–F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he was a Ph.D. Student with Aalborg University, Aalborg, Denmark. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has received 15 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was an Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011.

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