Nanoscale RF CMOS Transceiver Design

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Optimum Region for RFIC Design?

- Aggressive CMOS technology scaling down to 28 nm.
- RFICs under low voltage/power operation.
- Suitable region for RFIC design ?
- High overall performance w. min. power consumption.

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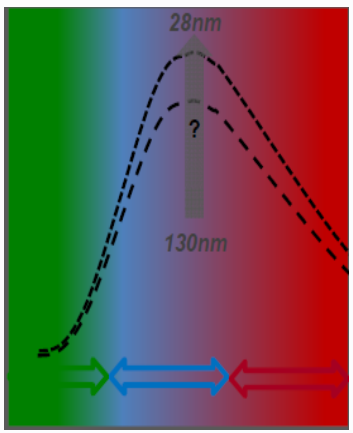

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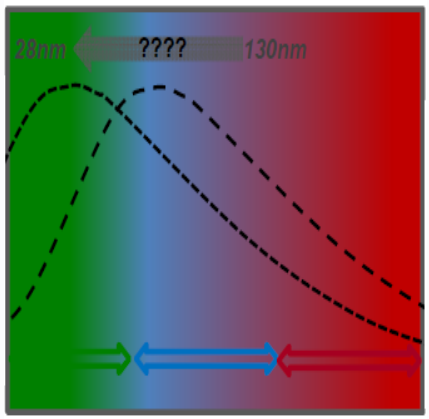

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- Channel noise models for transistors working in these regions
- Scaling issues of the active noise sources research area for future studies.

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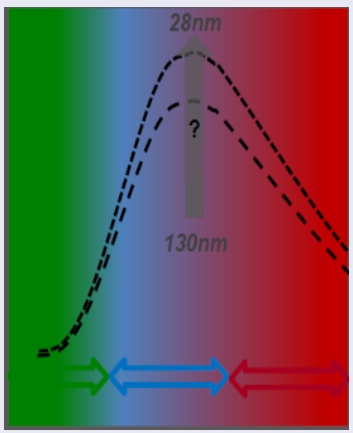

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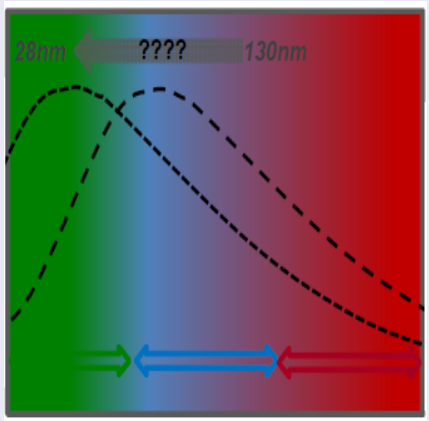

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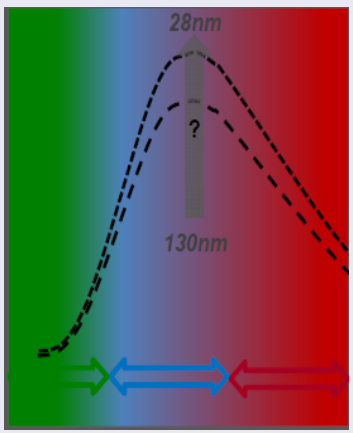

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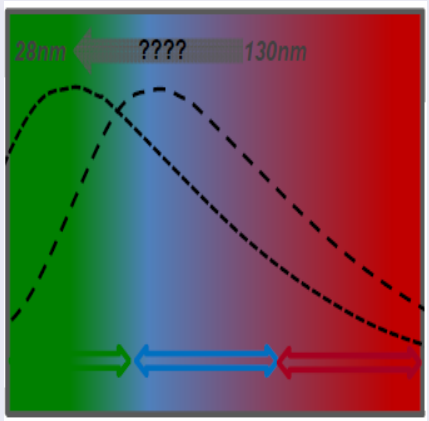

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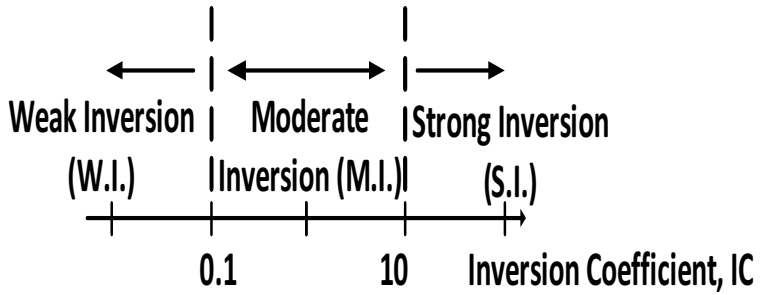
- Simple and easy to evaluate.
- Thermal noise in terms of RFIC design
- Validation through RFIC design



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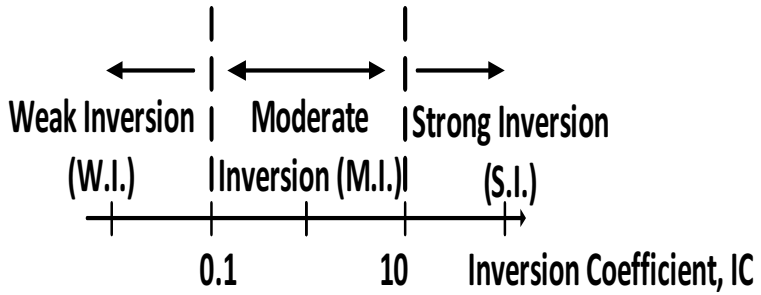

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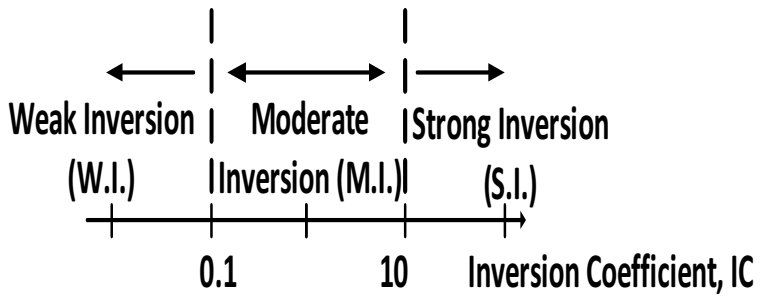

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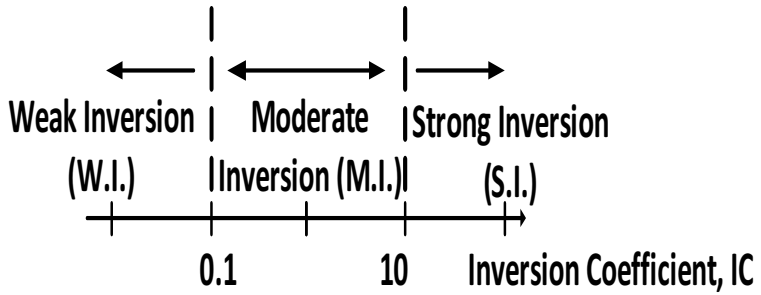

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System to Block

- Receiver blocks

Device Level

- Tapeout of an RF Test Chip in 90nm CMOS
  - Measurements and De-embedding
- Small-signal analysis
  - Figures of Merit (FoM) for LNA Design
- Thermal Noise
  - RF noise trends
  - Noise parameters essential for LNA design
- Verification with EKV3 model

Circuit Level

- LNA Topologies

Circuit Level

- 30 GHz LNA
- 5 GHz LNA based on FoM

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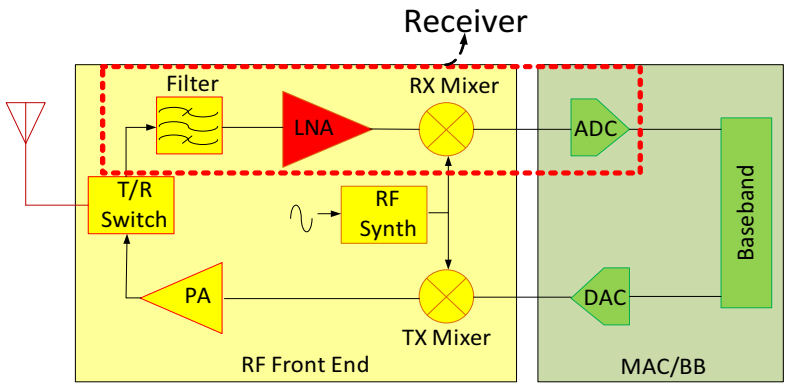

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  - Heterodyne (IF, problem of image)
  - Direct conversion (zero IF)
- Noise of cascaded stages
  - $NF = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{P1}} + \frac{NF_m - 1}{A_{P1} \cdots A_{P(m-1)}}$
- Non-linearity of cascaded stages
  - $\frac{1}{A^2_{IIP3}} = \frac{1}{A^2_{IIP3,1}} + \frac{\alpha_1^2}{A^2_{IIP3,2}} + \frac{\alpha_1^2 \beta_1^2}{A^2_{IIP3,2} A^2_{IIP3,3}}$
- LNA should provide
  - Minimum noise figure
  - Moderately high gain, depending on the application

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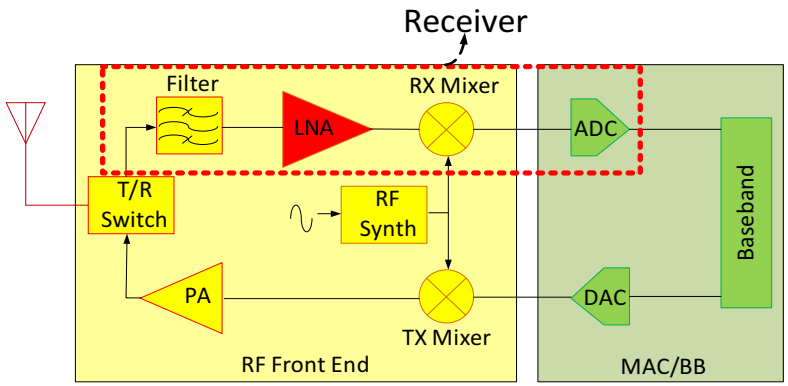

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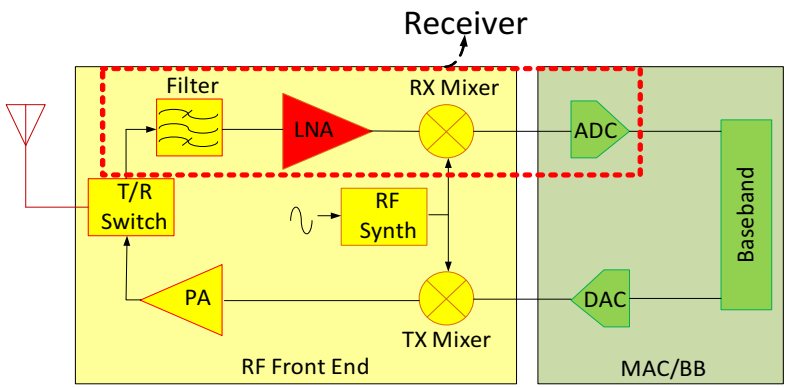

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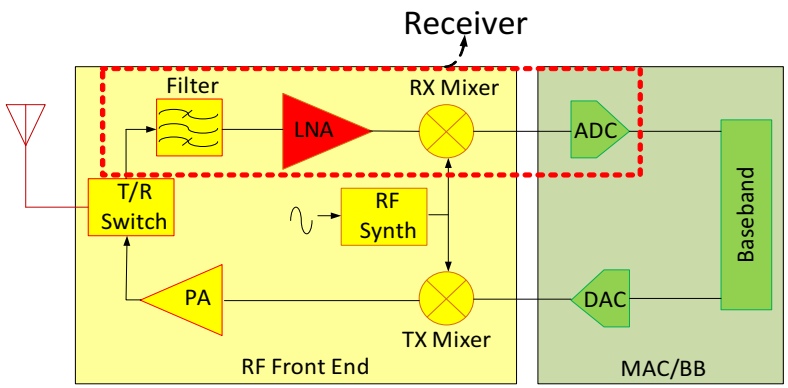

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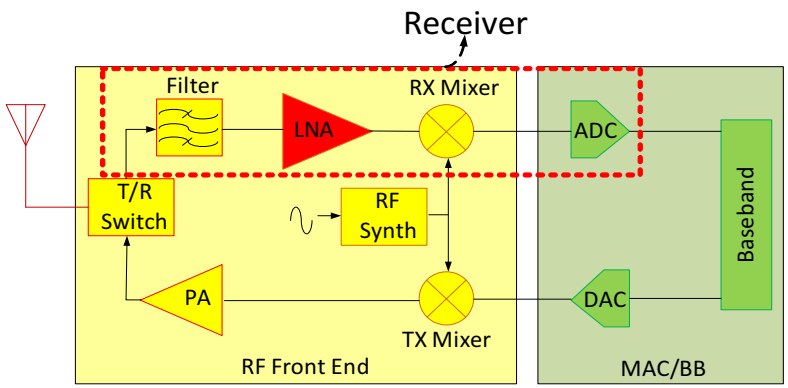

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LNA Requirements

Matching

- Power matching
- Maximum power transfer to a load
  - $Z_L = Z_S^*$
- Input matching
  - Input impedance equal to 50 Ω
  - Return loss: $\Gamma = \frac{Z_{in}-R_S}{Z_{in}+R_S}$
  - Ideally $\Gamma = 0$
- Noise matching
  - $Y_S = Y_{opt}$

Stability and Reverse Isolation

- Feedback paths from the output to the input may lead to instability
- Stern stability factor
  - $K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}||S_{12}|}$
  - When K>1 and Δ<1 the circuit is unconditionally stable
- Reverse isolation (-S_{12})
  - Improves stability
  - Reduces spurious LO tone at the antenna

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Power Gain

- Voltage gain, A_V should be optimized
- When $Z_{in} = Z_{out}$, $A_V = A_P$
- Several types of power gain

Noise

- Noise factor
  - $F = SNR_{in}/SNR_{out}$
  - Ideally $F = 1$
  - $NF = 10logF$
- Should be kept minimum

Power Dissipation

- LNA consumes a small fraction of the overall RX power
- However power dissipation should be minimized
- P_{cons} has to be considered along w. the other FoM

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LNA topologies

- Widely used LNA Topologies
  - Common Gate (CG)
  - Common Source (CS) (w. resistive feedback)
  - CS w. thermal noise cancellation
  - Cascode w. inductive degeneration
  - Transformer feedback
- Certain pros and cons
- Circuit topology dictated by the specific application the LNA has to serve

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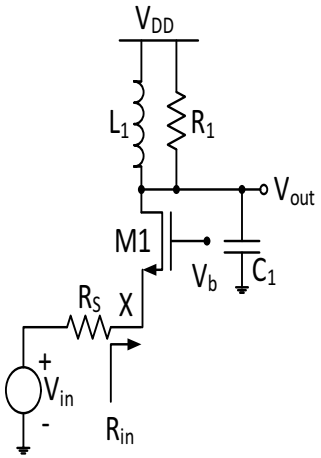
Common Gate LNA

CG Stage w. Inductive Load

- Input impedance
  - $1/g_{ms}$
- Voltage gain
  - $A_v \equiv \frac{V_{out}}{V_{in}} = \frac{R_1}{2R_S}$
- Thermal noise
  - $F = 1 + \gamma + 4\frac{R_S}{R_1}$



Limitation

- Even if $4\frac{R_S}{R_1} \ll 1 + \gamma$, for γ=1, NF=3 dB
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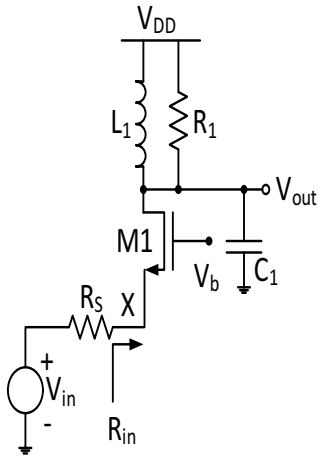

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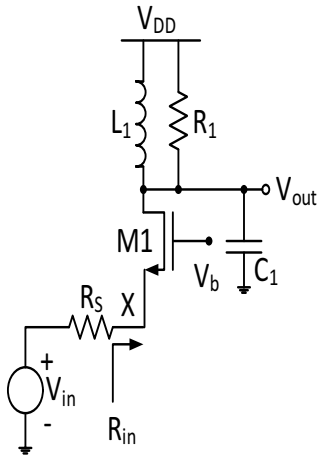

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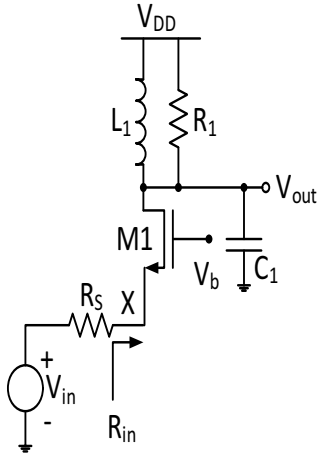

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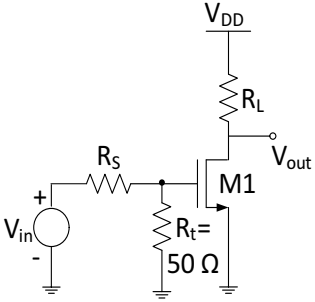
Common Source LNA

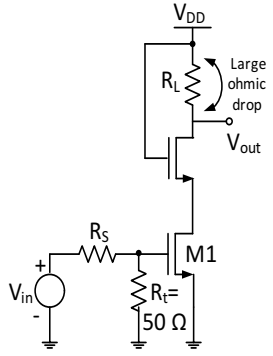
CS Stage

- CS topology w. resistive load
- Capacitive input impedance
  - $Z_{in} = \frac{R_S}{1+\frac{j\omega}{\omega_p}}$, $\omega_p = \frac{1}{R_S(C_{gs}+MC_{gd})}$
  - Miller factor, $M = 1 + g_{m1} R_L$
- Capacitive feedback from output to input through C_{gd}
  - Poor reverse isolation



Cascode Stage

- Cascode topology w. resistive load
- Suffers from low gain
  - $R_L < \frac{V_{DD}-V_{DS,sat1}-V_{DS,sat2}}{I_D}$
  - For $V_{DS,sat} = 0.25V$, and $V_{DD} = 1.2V$, $A_V = 15dB$
- Replace R_L with an inductor load



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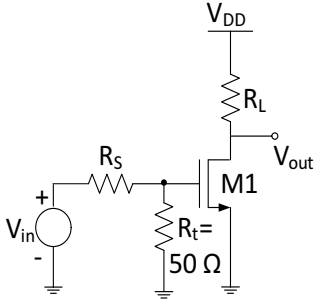

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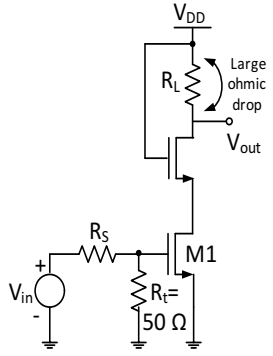
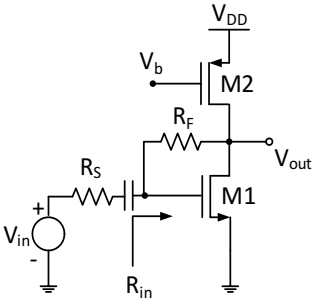


Common Source LNA

CS Stage w. Resistive Feedback

- R_F senses the output voltage and returns a current to the input
- Capacitive component due to C_{gs} still present
- R_F contributes to noise
  - $F = 1 + 4\frac{R_S}{R_F} + \gamma(g_{m1} + g_{m2})R_S$
  - NF exceeds 3 dB



CS Stage w. Noise Cancellation

- Based on CS w. resistive feedback
- Noise currents at points X and Y have equal sign
- Signal voltages at X and Y have opposite signs
- Noise cancellation
  - $V_{out,n} = V_{Y,n} - V_{X,n}A_V \Rightarrow A_{vc} = \frac{V_{Y,n}}{V_{X,n}} = 1 + \frac{R_F}{R_S}$
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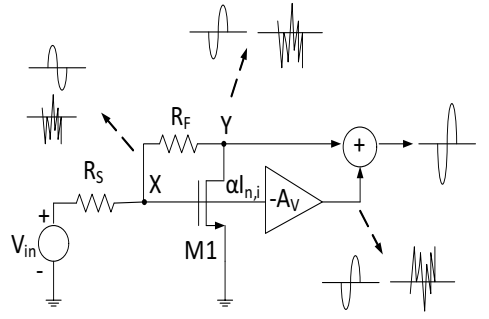

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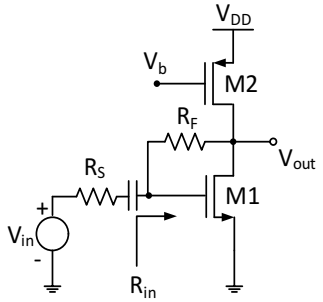

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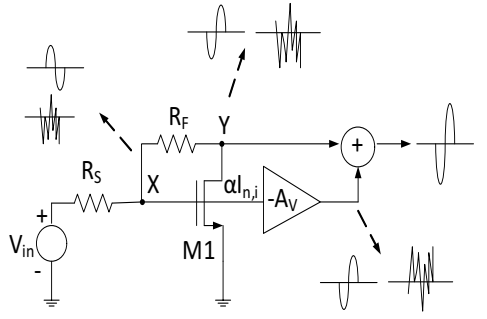

Transformer Feedback LNA

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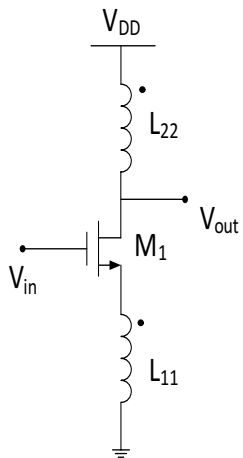
- C_{gd} canceled through an additional path from output to input
- Cancellation when
  - $\frac{n}{k} = \frac{C_{gs}}{C_{gd}}$
  - $n = \sqrt{L_{22}/L_{11}}$
  - $k = M/\sqrt{L_{11}L_{22}}$
- L_{11} used for source degeneration as well
- k affects gain, input and output impedance
  - Complex equations



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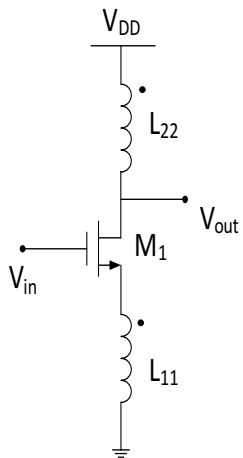
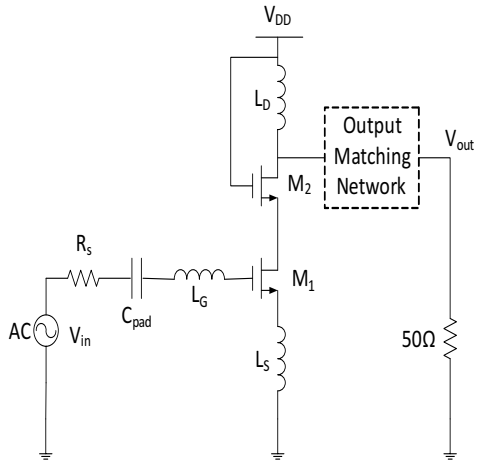


Cascode LNA w. Inductive Degeneration

Cascode Stage w. Inductive Degeneration

- Input impedance
  - $Z_{in} = \frac{1}{sC_{gs}} + s(L_S + L_G) + \omega_T L_S$
  - L_S is chosen so that $Real(Z_{in}) = 50\,\Omega$
  - L_G is chosen so that $Imag(Z_{in}) = 0$
  - Z_{in} purely reactive at ω_0
- Voltage gain
  - $A_V \equiv \frac{V_{out}}{V_{in}} = \frac{\omega_T}{2\omega_0} \cdot \frac{R_L}{R_S}$
  - Improves w. technology scaling
- Noise factor
  - $F = 1 + g_m \gamma R_S (\frac{\omega_0}{\omega_T})^2$
- Power constrained noise optimization
  - $W_{opt,P} \simeq \frac{1}{3\omega L C_{ox} R_S}$
- Power constrained simultaneous noise impedance matching (SNIM)
  - Extra capacitance in parallel w. C_{gs}



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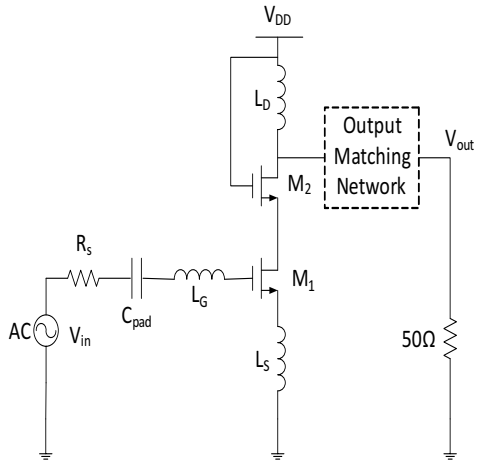
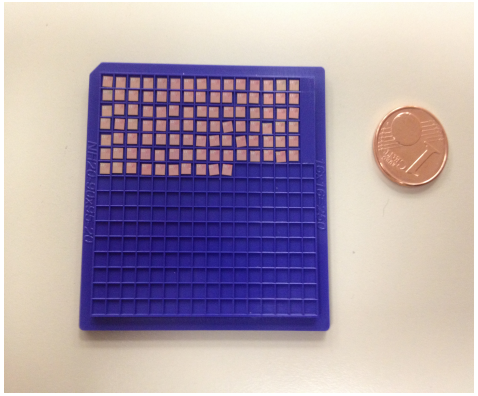
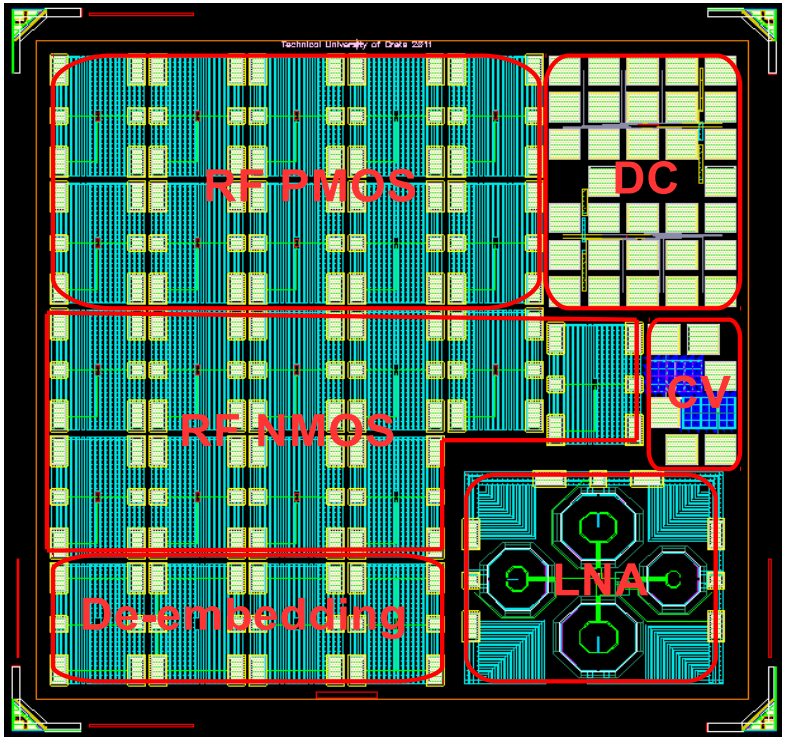


Tapeout of an RF Test Chip





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  - Chip area $3.5mm^2$
- RF structures
  - 10 n-MOS, 10 p-MOS
  - Multifinger
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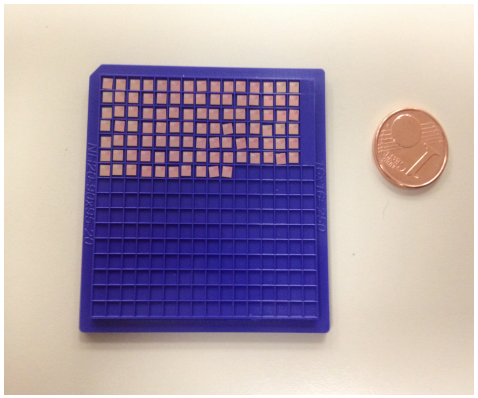

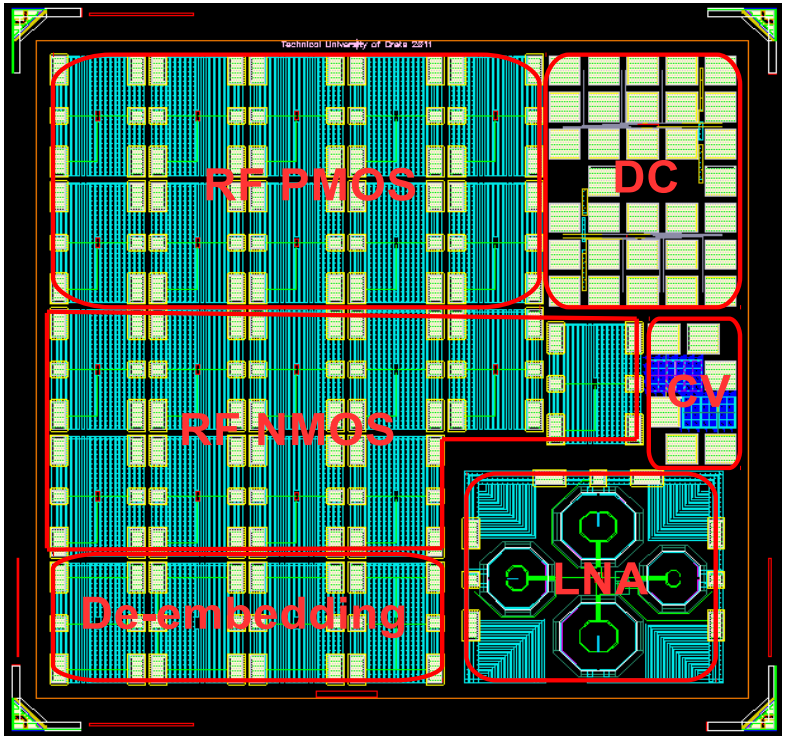

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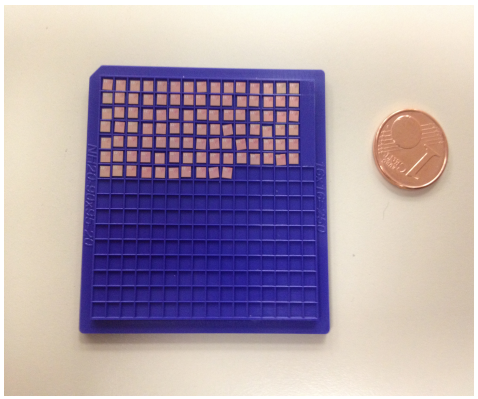

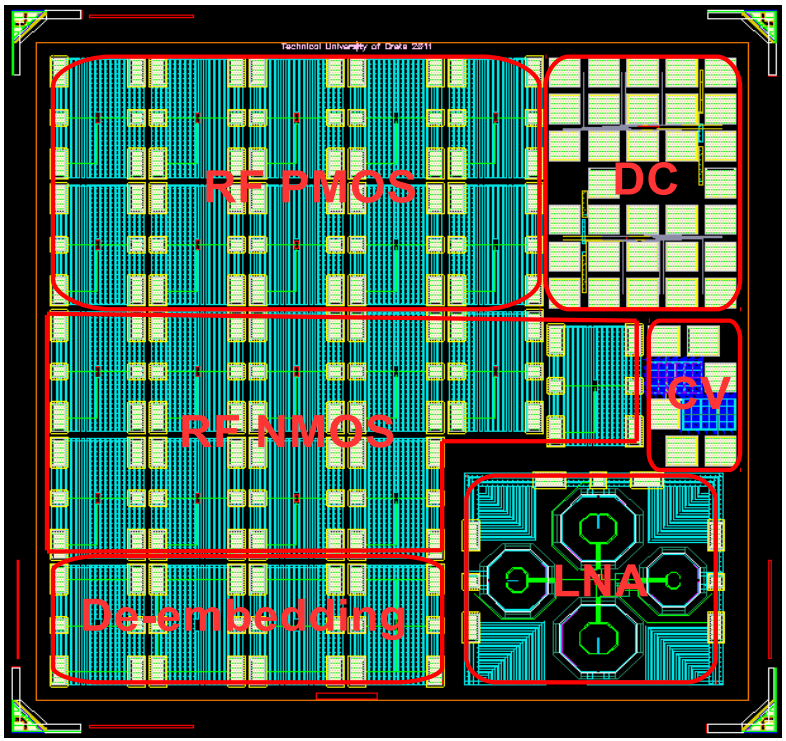

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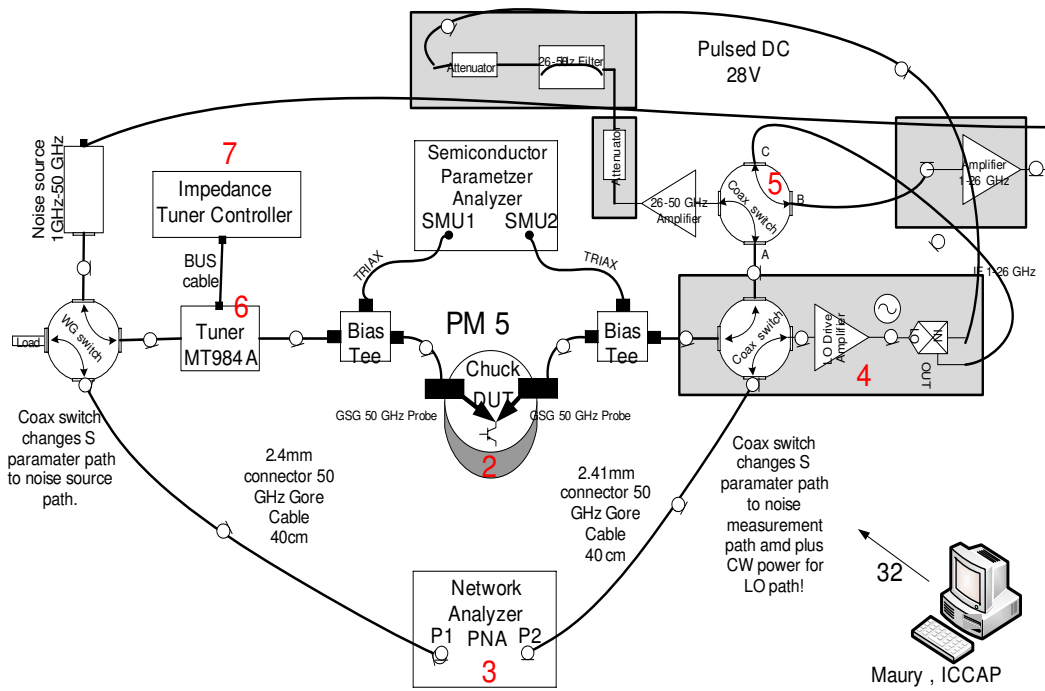
RF and Noise Measurements

Schroter & Sakalas, TU Dresden

CEDIC Laboratory Master plan Part 2

Prober PM 5: High frequency standard and special measurements

RF, DC and Noise 8 -50 GHz noise/lopad pull measurement system



1. Noise Figure meter , Spectrum analyzer Agilent E 4448 A
2. PM 5
3. PNA 8361 C
4. RF switch, LNA, downconverer
5. RF switch
6. Tuner Maury MT 984A 8-50 GHz
7. Impedance Tuner controller
8. Set of waveguides (missing, SFB)
9. 75-110GHz WG-Coax adapter x 2 (missing, SFB)
10. 75-110 GHz waveguide probes with BT (missing)
11. 75-110 GHz wg switch x2 (missing)
12. 75-110 GHz isolator x2 (missing)
13. 1GHz RF Gore cable x 2 (40cm) missing
14. 75-110 GHz load (missing)
15. RF power amplifier (75-110 GHz) missing
16. LNA for noise parameter (NP) meas. (missing)
17. Downconverter for NP meas. 75-110 GHz to 1-26 GHz (missing)

RF and Noise De-embedding

- RF De-embedding
  - Intrinsic performance of Device Under Test (DUT)
  - Improved three-step de-embedding (Vandamme et al., TED 2001)
- Noise De-embedding
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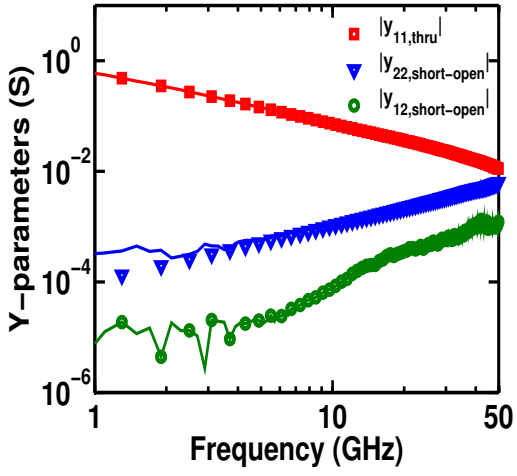

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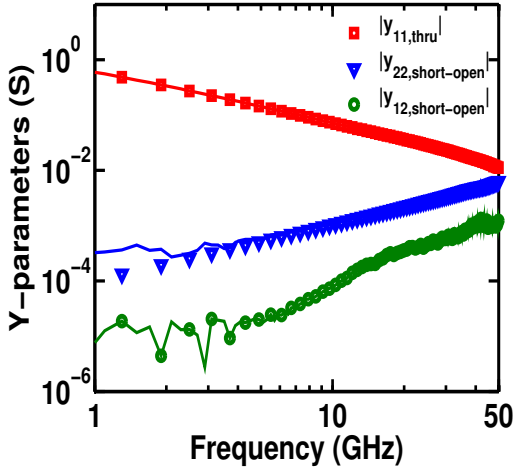

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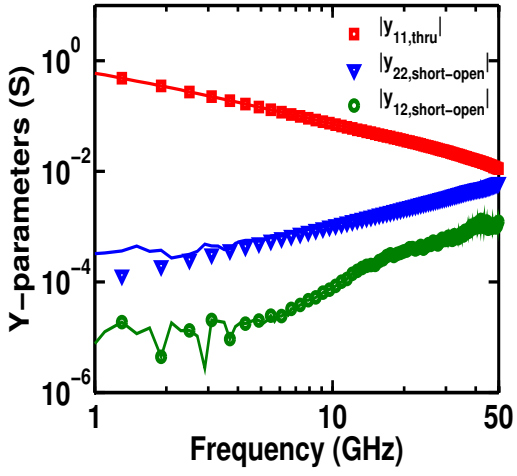

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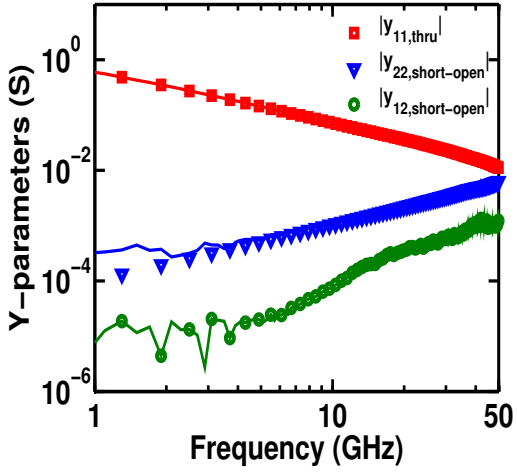

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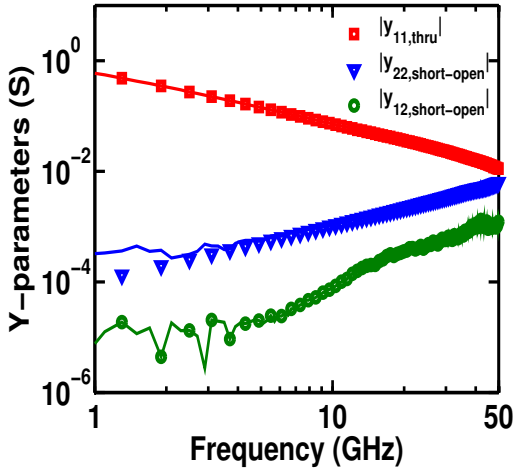

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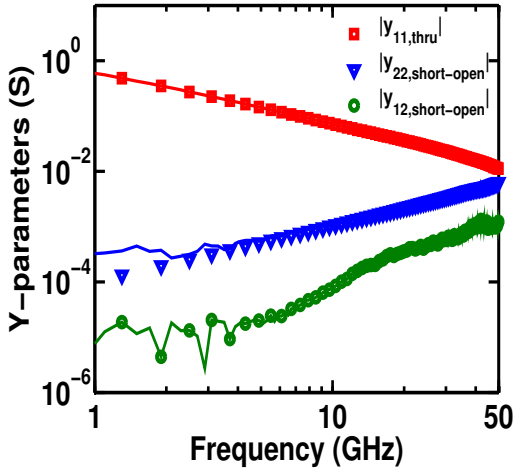
  - Cascade configuration (Chen et al., TED 2001)
- Verification



RF and Noise De-embedding

- RF De-embedding
  - Intrinsic performance of Device Under Test (DUT)
  - Improved three-step de-embedding (Vandamme et al., TED 2001)
- Noise De-embedding
  - Noise characteristics of the DUT
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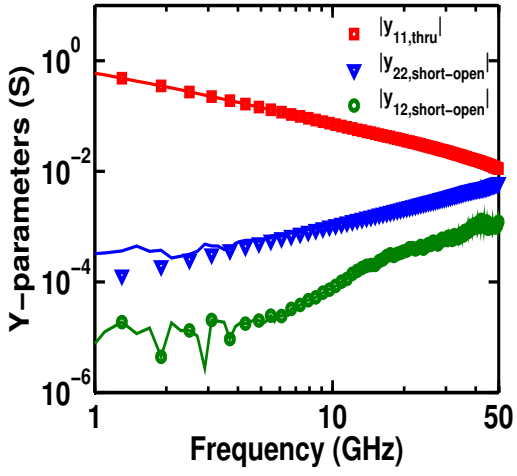
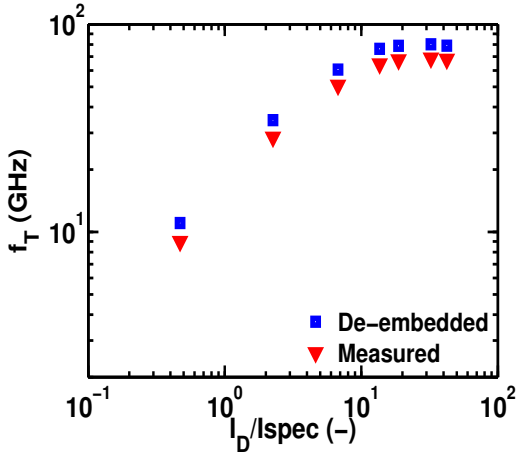
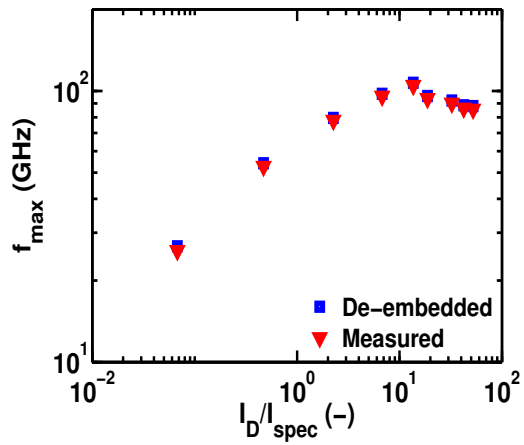
- Verification



RF De-embedding Results

- NMOS ($L = 100nm,\ W = 40x2um,\ V_{GS} = 0.65V,\ V_{DS} = 1.2V$)





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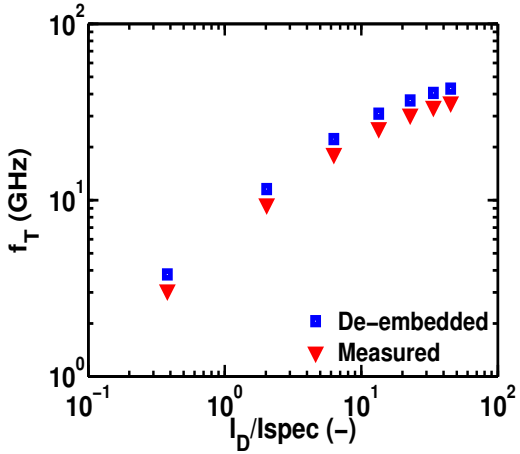

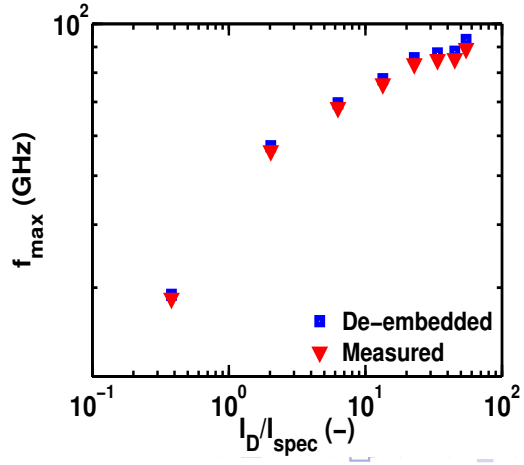

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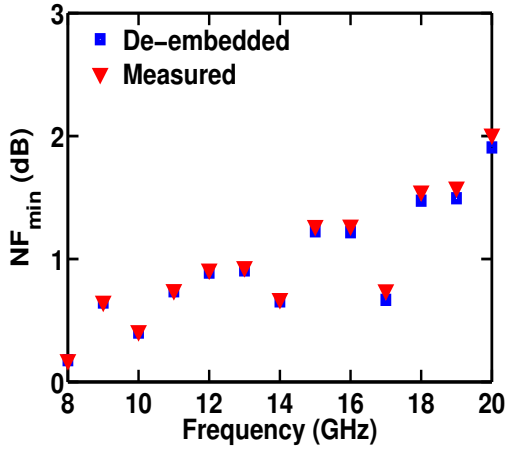

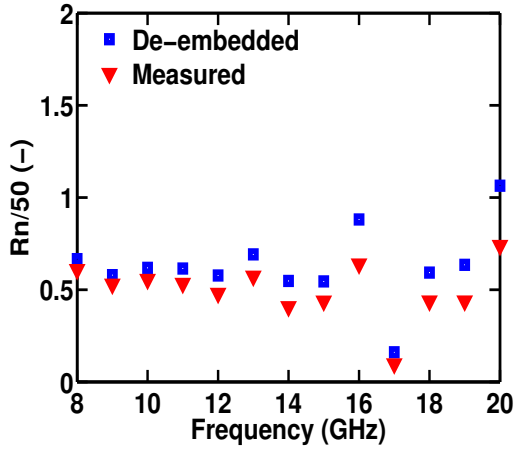

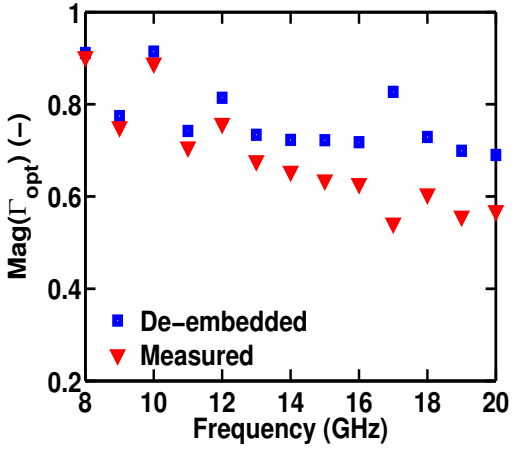

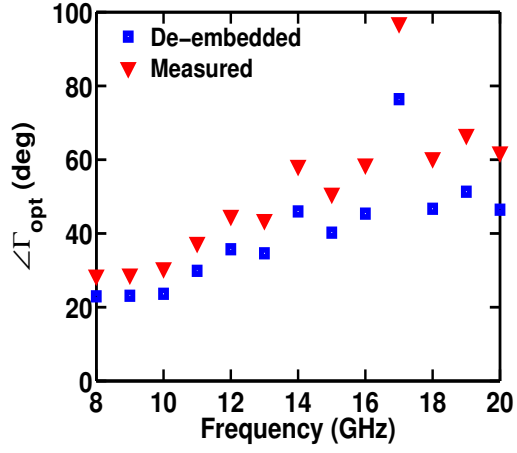

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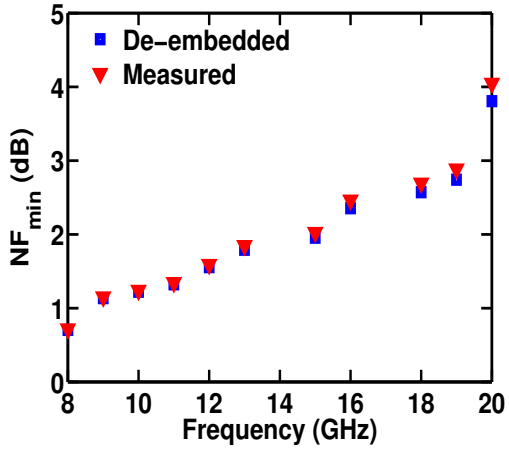
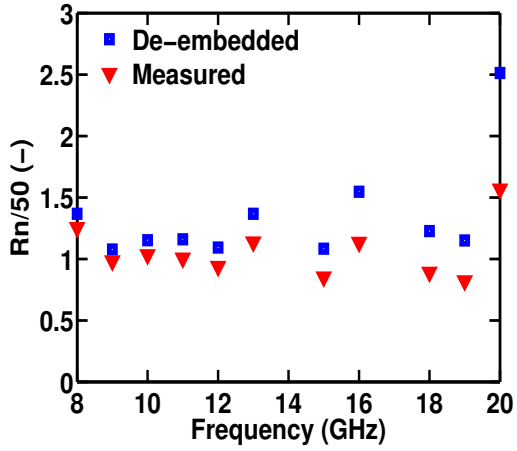
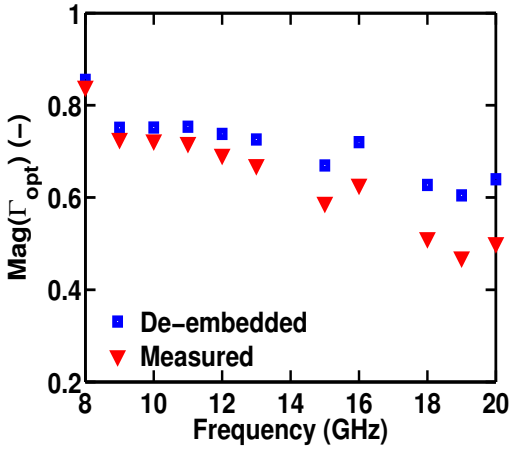
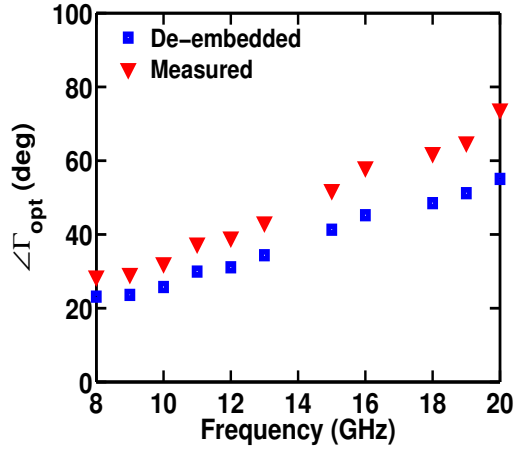




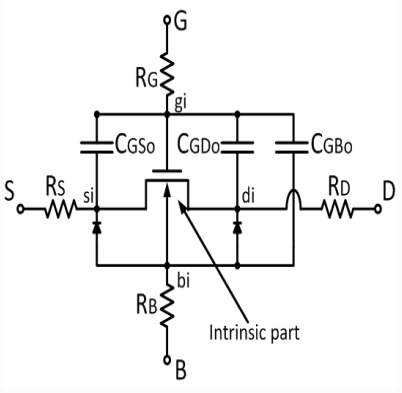




HF Modeling

- With frequency increase design characteristics start to degrade
  - Gain, NF_{min}
- At frequencies well below f_T
  - (Quasi) Static operation
  - Immediate current response to every voltage change
- Above quasi-static frequency, Ω_{qs}
  - Charges need time to adjust to voltage changes
  - Charge density dependent on the past voltage values
- Ω_{qs} stands as a FoM
  - Frequency the device can reach wo. accounting for the extrinsic components
- Performance degradation when Ω_{qs} 5-7 times higher than f_0

- MOS extrinsic part
  - Significant w. frequency increase
- Connection between intrinsic and extrinsic parts
  - Source-drain extensions
  - Parasitic resistances R_S and R_D
- Simple equivalent circuit
  - Experiences limitations



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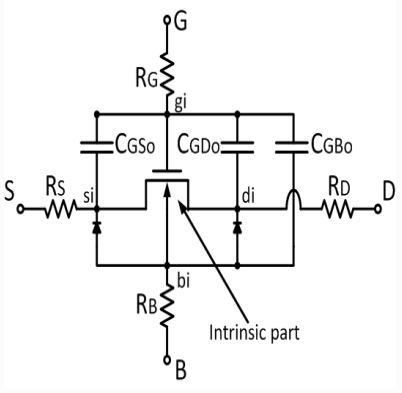

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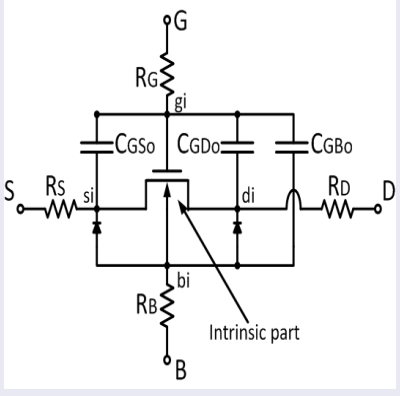

Y-Parameters

- Y-parameters: convenient way to extract FoM and device parameters
  - $Y_{11} \cong \omega^2 R_G C_G^2 + j\omega C_G$
  - $Y_{12} \cong -\omega^2 R_G C_{GD} C_G - j\omega C_{GD}$
  - $Y_{21} \cong G_m - \omega^2 R_G C_G (C_{GD} + C_m) - j\omega (C_{GD} + C_m)$
  - $Y_{22} \cong G_{ds} + \omega^2 R_G (C_G C_{BD} + C_G C_{GD} + C_{GD} C_m) + j\omega (C_{BD} + C_{GD})$
- $C_G = \frac{Imag(Y_{11})}{\omega}$
- $C_{GD} = \frac{Imag(Y_{12})}{\omega}$
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f_T, f_{max} and G_m/I_D

- Unity gain frequency (f_T)
  - Frequency where current gain of a CS amplifier falls to unity
  - $f_T = \frac{f_{spot}}{Imag(\frac{Y_{11}}{Y_{21}})}$
  - Can be extrapolated from h_{21} in S.I., saturation, where the slope is $-20dB/dec$
- Maximum oscillation frequency (f_{max})
  - Calculated through unilateral gain
  - Maximum available gain assuming neutralized device
  - $U = \frac{|Y_{21}-Y_{12}|^2}{4[real(Y_{11})Real(Y_{22})-Real(Y_{12})Real(Y_{21})]}$
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  - $\frac{G_m U_T}{I_D} = \frac{2}{n(\sqrt{4IC+1}+1)}$
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FoM for LNA Design

$FoM_{(G_m/I_D)f_T}$

- Transconductance frequency product (TFP)
  - $TFP = (G_m/I_D) \cdot f_T$
  - Used to optimize low-power circuits (Mangla et al., MJ 2013)
  - Stands as a FoM for LNA design
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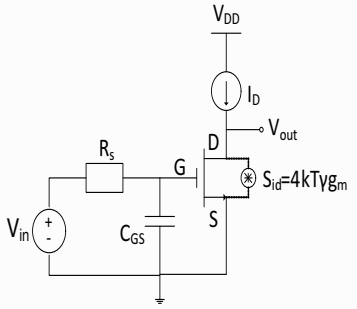

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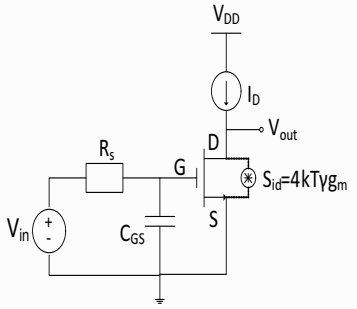

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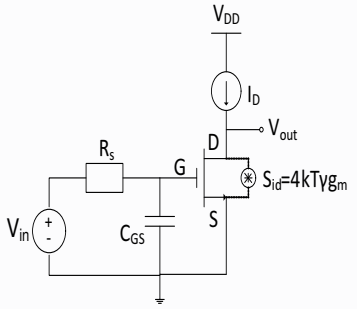

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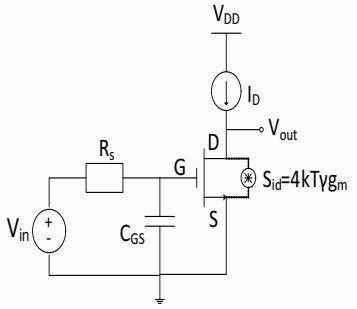

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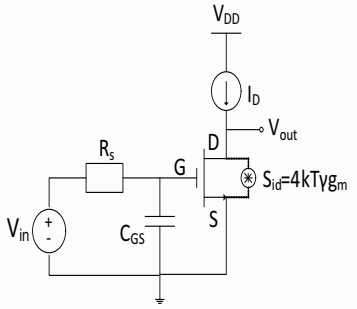

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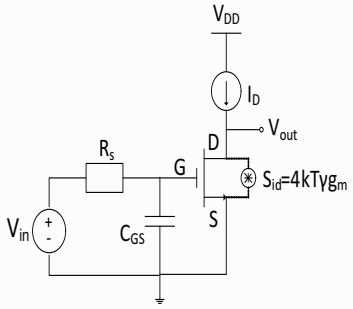

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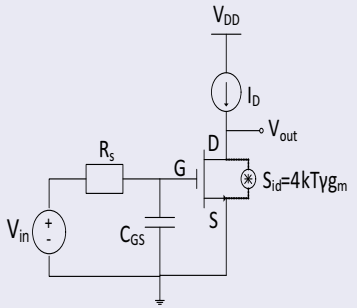

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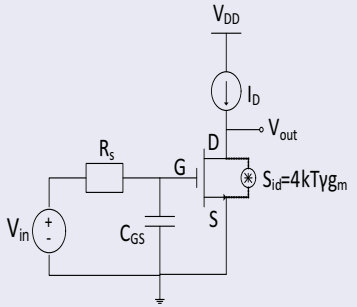

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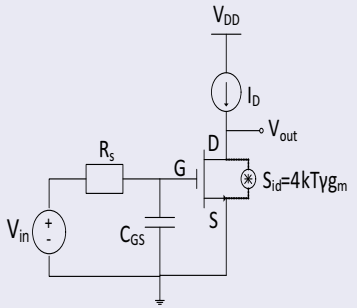

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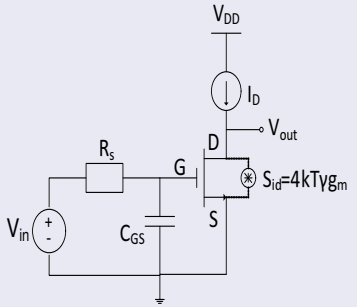

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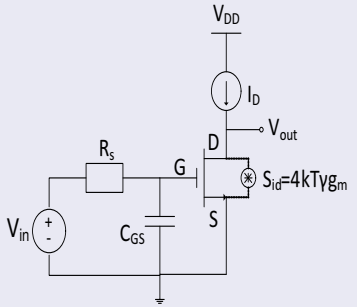

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- Representative of cascode topology
- Easy to evaluate from DC measurements
- Has not been studied w. length scaling

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- Combines TFP w. intrinsic voltage gain
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- Non-linearities expressed through
  - Harmonics
  - Intermodulation (two-tone test)
- Mainly due to the non-linear I_D-V_G characteristic
  - $G_m = \frac{\partial I_D}{\partial V_{GS}}$, $G_{m2} = \frac{\partial^2 I_D}{\partial V_{GS}^2}$, $G_{m3} = \frac{\partial^3 I_D}{\partial V_{GS}^3}$
- Metrics
  - $P_{1dB} = \left| \frac{G_m}{13.8 G_{m3} R_S} \right|$
  - $P_{IP3} = \left| \frac{2 G_m}{3 G_{m3} R_S} \right|$
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- FoM presented versus
  - Measured data for the 90 nm case
  - TCAD data for technology nodes of L=180, 90, 45, 22 nm
  - Verified w. EKV3
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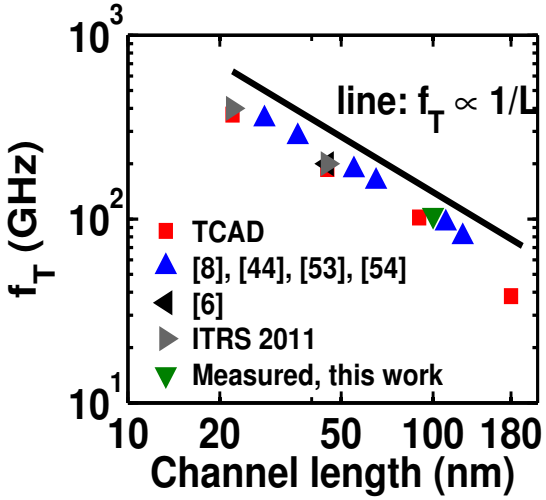

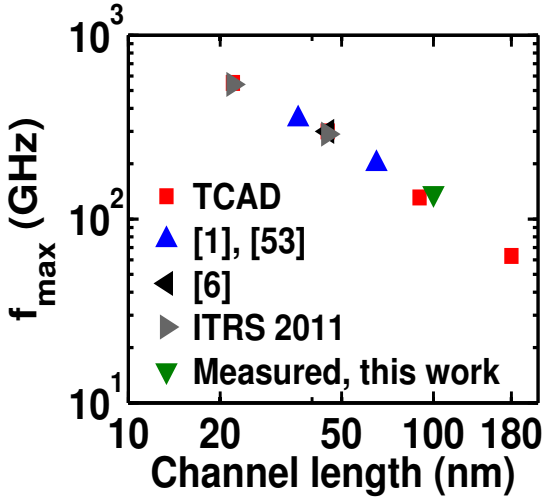

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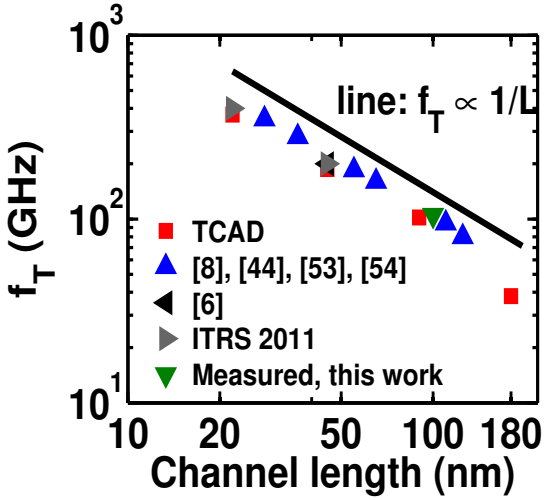

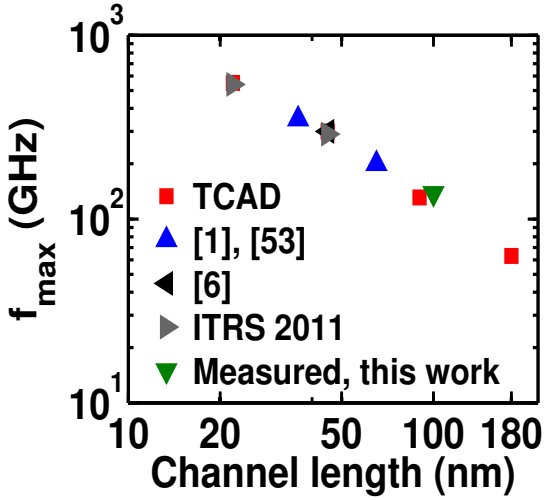

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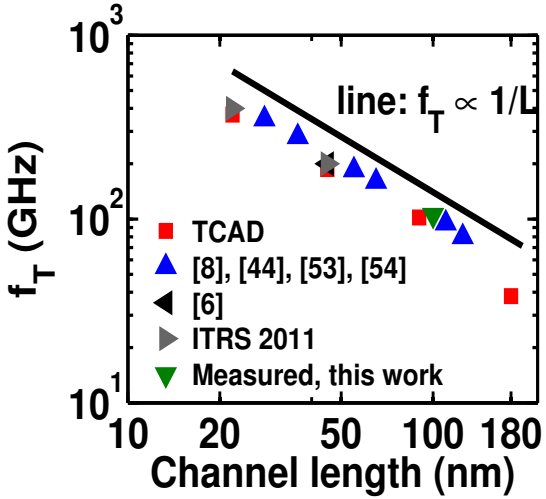

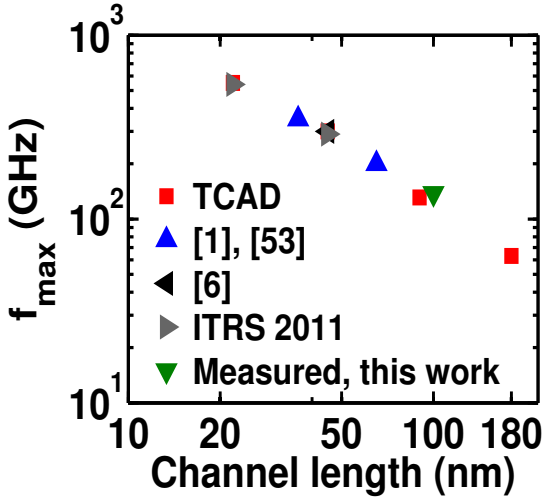

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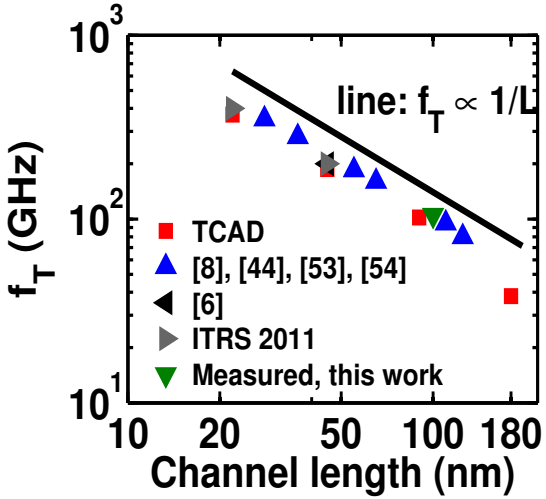

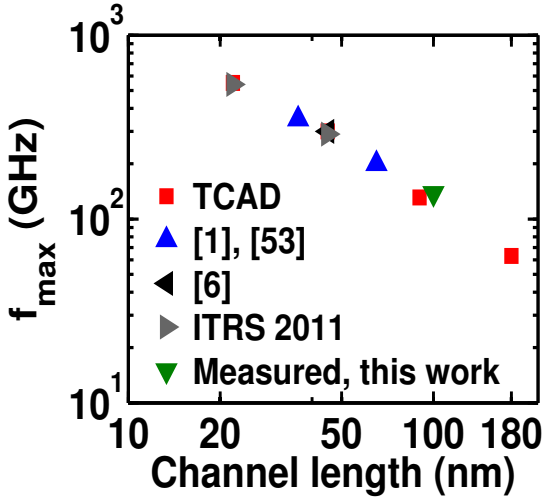

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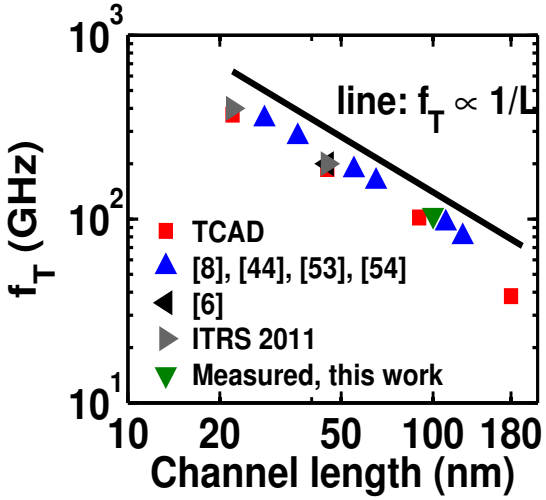
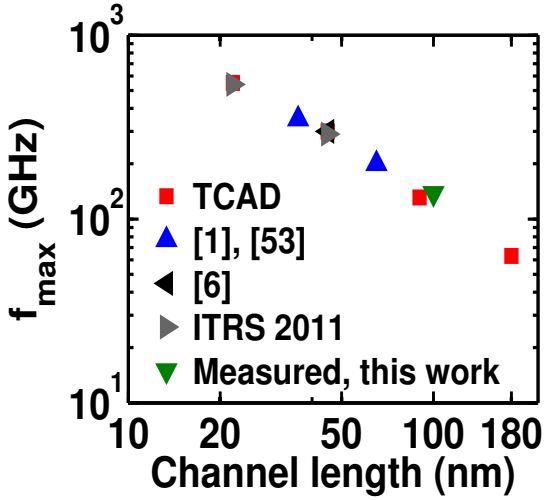
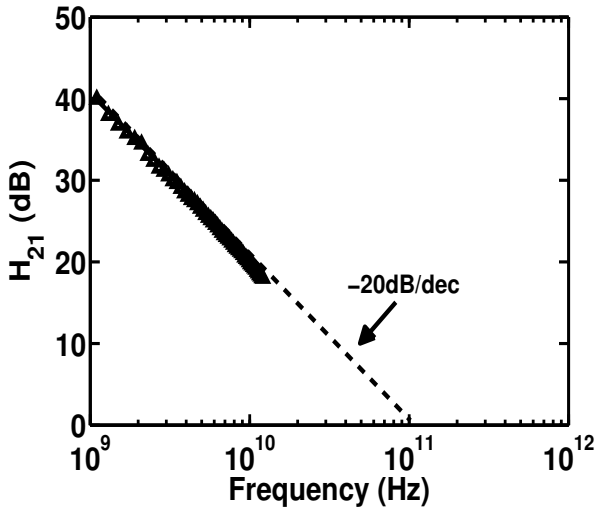


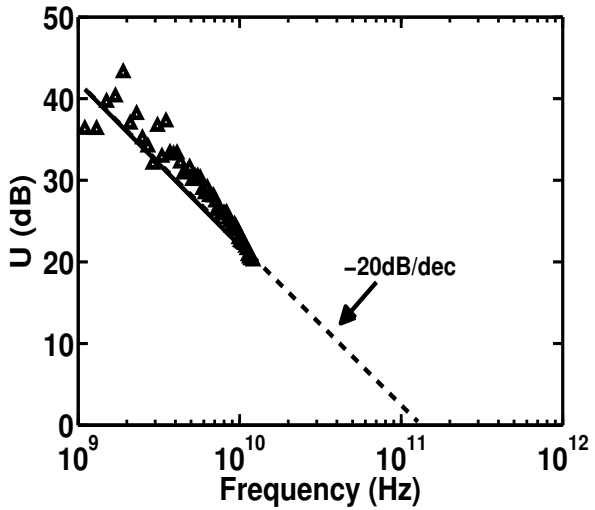


Antonopoulos et al., TED, 2013

h_{21} and U

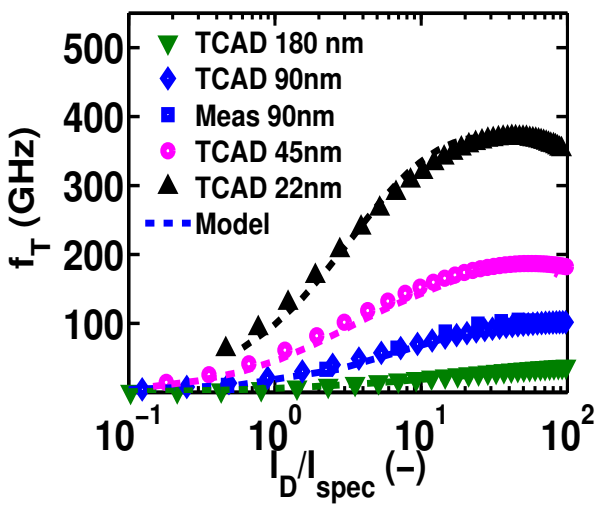
- Measured ($L = 100nm$, $W = 10x2um$, $V_{DS} = 1V$)

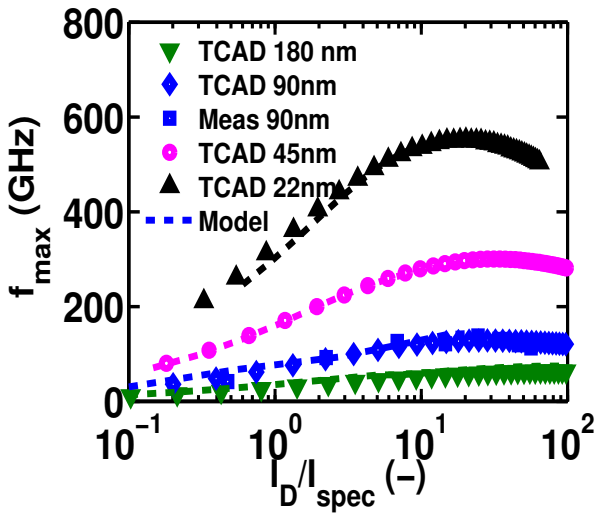




f_T and f_{max}

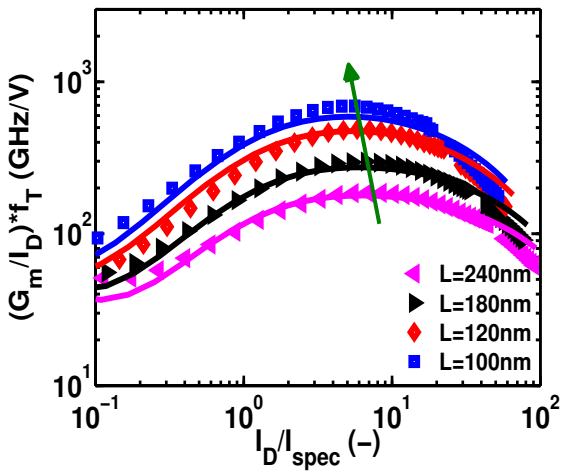
- TCAD and measured ($W = 10x2um$, $V_{DS} = 0.9V$)

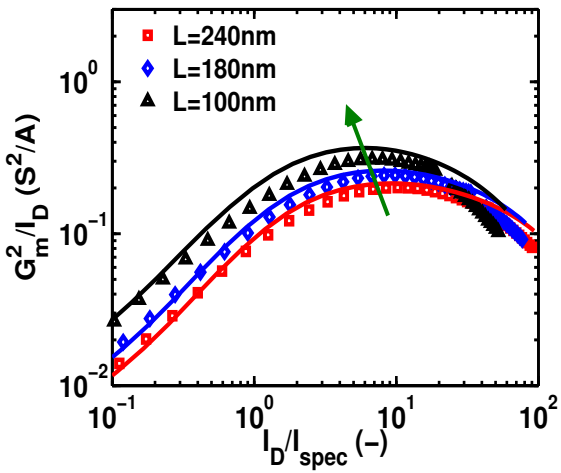


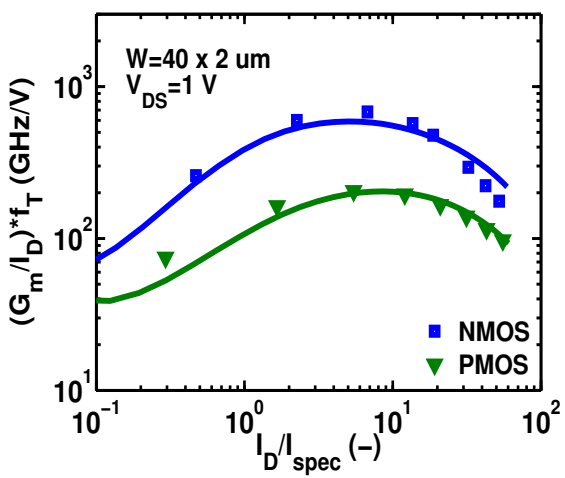


$(G_m/I_D)f_T$ and G_m^2/I_D

- Measured ($W = 40x2um$, $V_{DS} = 1V$)

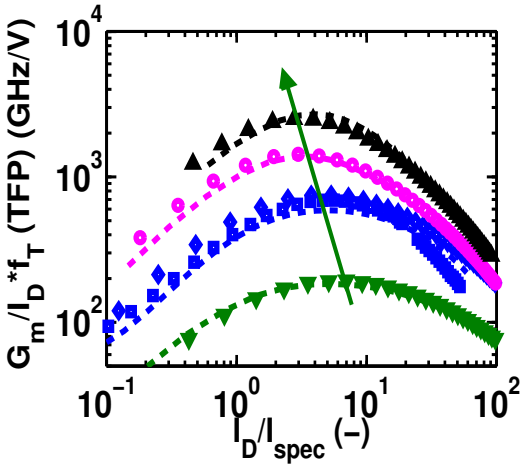


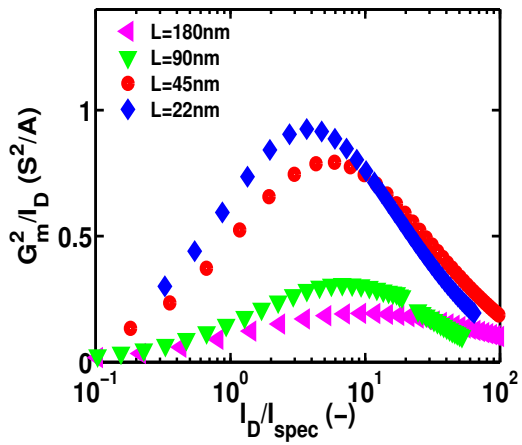


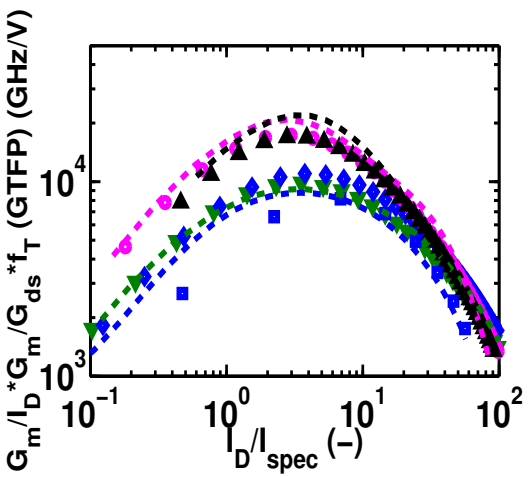


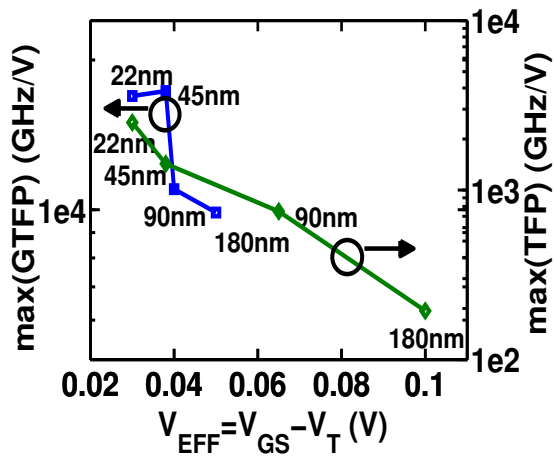
$(G_m/I_D)f_T$, G_m^2/I_D and GTFP

- TCAD and measured ($W = 10x2um$, $V_{DS} = 0.9V$)



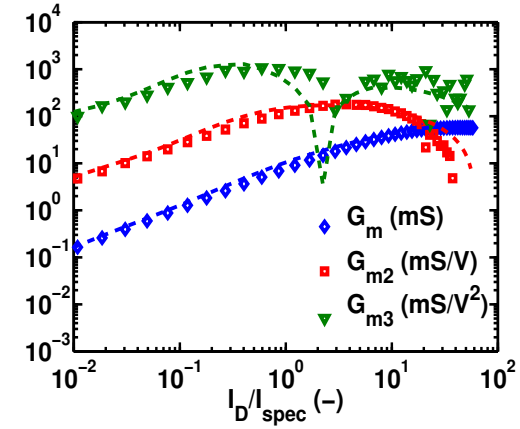


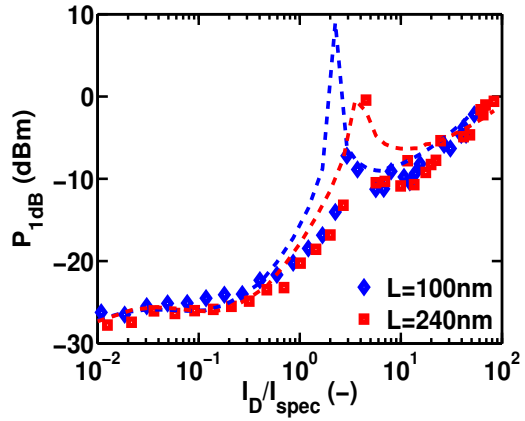


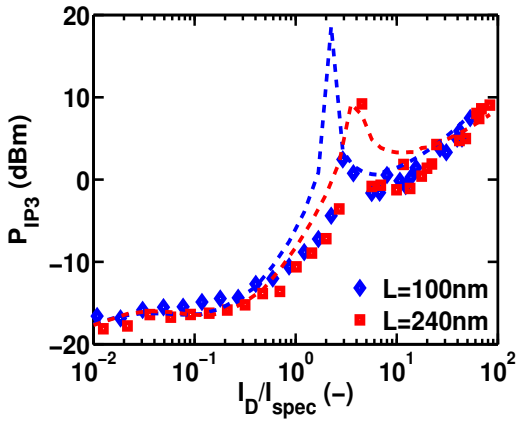


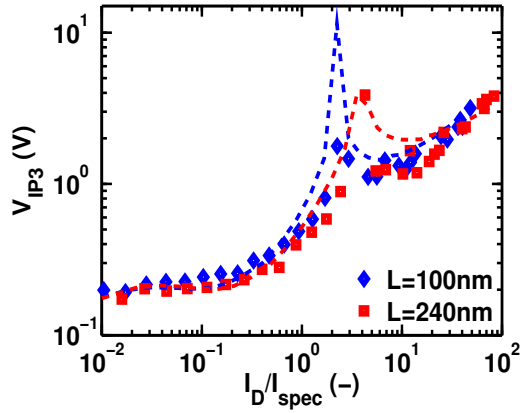
Non-Linearities

- Measured ($W = 40x2um$, $V_{DS} = 1V$, $@f = 1.1GHz$)









Antonopoulos et al., RFIC Symp., 2013

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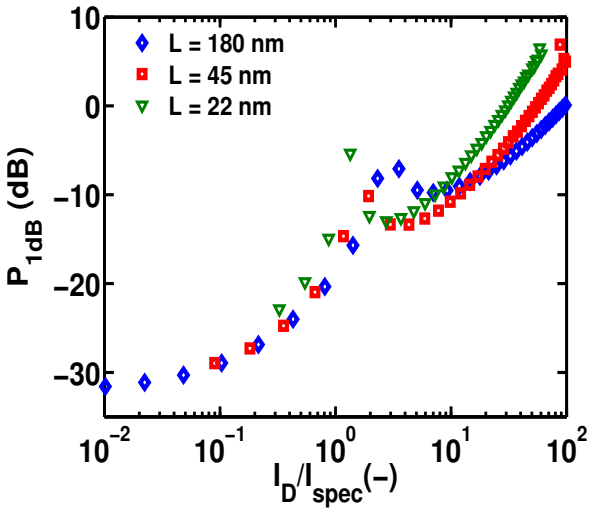

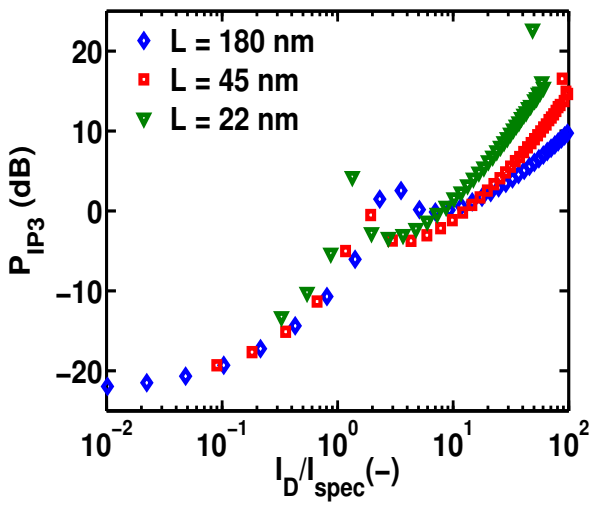

Conclusions on Small-Signal Analysis and LNA Performance

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  - Bias, L, and technology
- Individual FoM show a shift to lower inversion level w. length scaling
- Combined FoM show the same shift
- Optimum LNA performance studied via $(G_m/I_D) \cdot f_T$ and G_m^2/I_D
  - Experience the same behavior
  - Optimum value achieved in M.I.

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- Optimum RF performance shifted toward around-threshold operation as planar bulk CMOS scales down to 22 nm

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Noise in Semiconductors

- Random process
  - Even if the past values are known, the instantaneous value cannot be predicted
- Power spectral density
  - Characterizes the average power the signal carries
- Noise in a resistor: Representations
  - Norton equivalent: $S_{v_n}(f) = \overline{V_n^2} = 4kTR_1\,(V^2/Hz)$
  - Thevenin equivalent: $S_{I_n}(f) = \overline{I_n^2} = \overline{V_n^2}/R_1^2 = 4kT/R_1\,(A^2/Hz)$
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- Hot research topic
  - Many groups (Birbas & Triantis, Enz & Roy, Schroter & Sakalas, Smit & Scholten, Deen & Chen,...)
- Compact models (BSIM, PSP, EKV)
  - Noise description as a function of geometry, bias, scaling
  - Controversies in literature
- Discrepancies
  - Excess noise in short devices and short channel effects (SCE)
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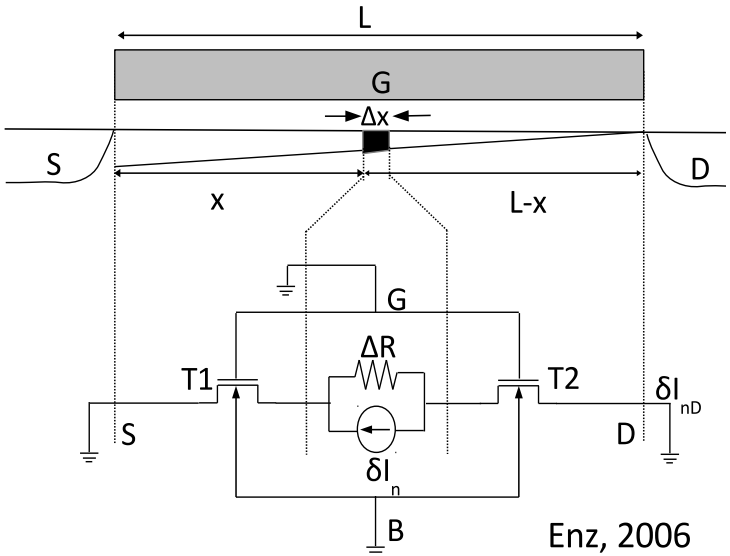
Thermal Noise in MOSTs: The EKV3 Model

- Thermal noise due to local random fluctuations of the carrier velocity
  - Transferred to the device terminals
  - Modeled as a random current added to the DC local current
- Modeling approach
  - Local noisy source
  - x and x+Δx from Source
  - L-x and L-(x+Δx) from Drain
  - Noisy current source in parallel with ΔR
  - Transistor is split into T1 and T2
  - Channel conductance: $\frac{1}{G_{ch}} = \frac{1}{G_1} + \frac{1}{G_2}$
  - Drain fluctuation due to local noise source: $\delta I_{nD} = G_{ch} \Delta R \delta I_n$
  - PSD of drain current due to all noisy sources:

    $S_{\Delta In_D^2}(\omega) = \int_0^L G_{ch}^2 \Delta R^2 \frac{S_{\delta I_n^2}(\omega, x)}{\Delta x} dx$
- Modeling approach applicable to frequencies well beyond f_T



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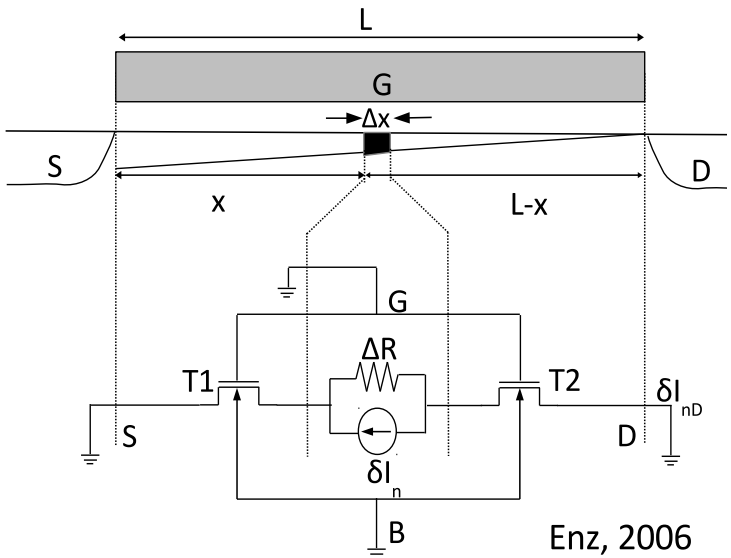

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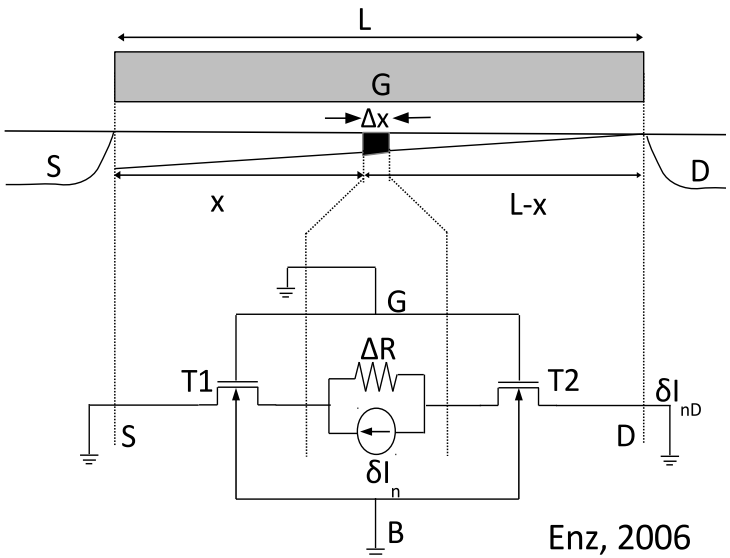

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Thermal Noise of Long Channel Devices

- Constant carrier mobility, μ
- PSD of drain noise current
  - $I_D = \mu W(-Q_i)\frac{dV}{dx}$
  - $G_{ch} = \frac{dI_D}{dV} = \mu(-Q_i)\frac{W}{L}$
  - $\Delta R = \frac{\Delta V}{I_D} = \frac{\Delta x}{W\mu(-Q_i)}$
  - Due to local noise source δI_n: $S_{\delta I_{nD}^2}(\omega,x) = G_{ch}^2(x)\Delta R^2(x) S_{\delta I_n^2}(\omega,x)$
  - Due to all noise sources: $S_{\Delta I_{nD}^2}(\omega) = \int_0^L (\frac{\Delta x}{L})^2 \frac{S_{\delta I_n^2}(\omega,x)}{\Delta x} dx = \frac{1}{L^2}\int_o^L \Delta x S_{\delta I_n^2}(\omega,x) dx$
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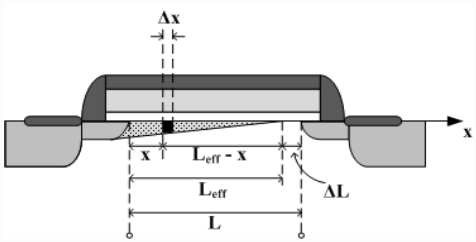
Short Channel Effects

Velocity Saturation (VS) and Carrier Heating (CH)

- Electrons and holes have a characteristic E_c and u_{sat}
- When E_x becomes comparable to E_c then u_{drift} starts to saturate
- High lateral electric field
  - Carriers gain higher energy
  - Random collisions w. lattice
  - Carrier temperature increases w. electric field
- VS and CH, interdependent phenomena
- EKV3 accounts for both
  - Critical field parameter
  - $\lambda_c = \frac{2U_T}{L_{eff}\, E_c}$
  - The higher the λ_c, the stronger the SCE

Channel Length Modulation (CLM)

- In S.I. as V_{DS} increases the channel pinches off
- Channel is split into two regions
  - Non-saturated region (L_{eff})
  - VS region, ΔL
- Carriers in VS region
  - Maximum velocity
  - Noise voltage fluctuations do not propagate to drain
- Only the active region contributes to channel thermal noise



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- Electrons and holes have a characteristic E_c and u_{sat}
- When E_x becomes comparable to E_c then u_{drift} starts to saturate
- High lateral electric field
  - Carriers gain higher energy
  - Random collisions w. lattice
  - Carrier temperature increases w. electric field
- VS and CH, interdependent phenomena
- EKV3 accounts for both
  - Critical field parameter
  - $\lambda_c = \frac{2U_T}{L_{eff}\, E_c}$
  - The higher the λ_c, the stronger the SCE

Channel Length Modulation (CLM)

- In S.I. as V_{DS} increases the channel pinches off
- Channel is split into two regions
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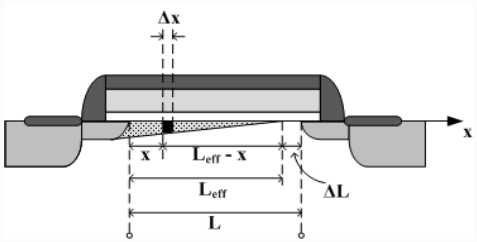

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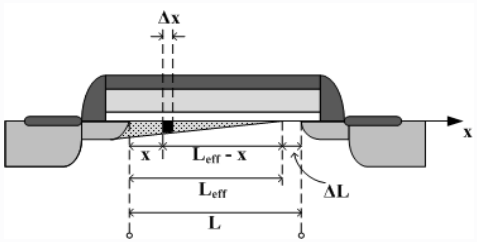

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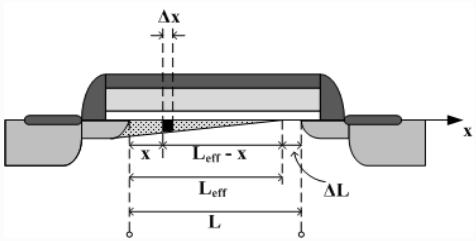

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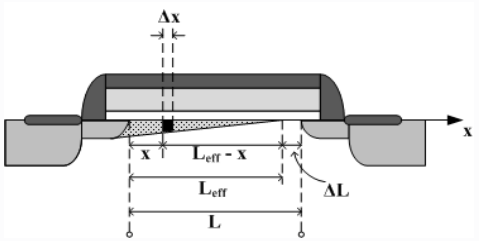

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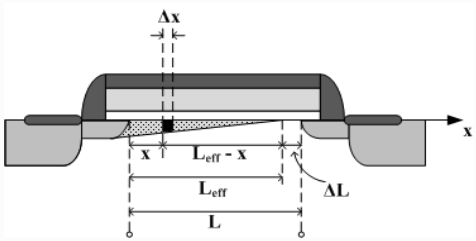

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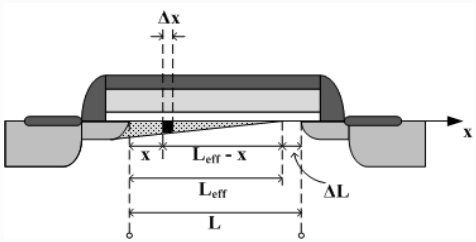

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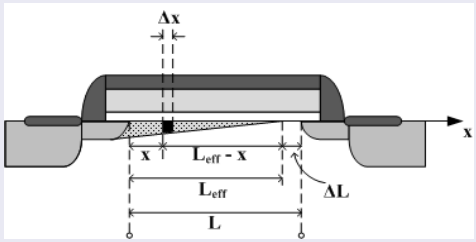

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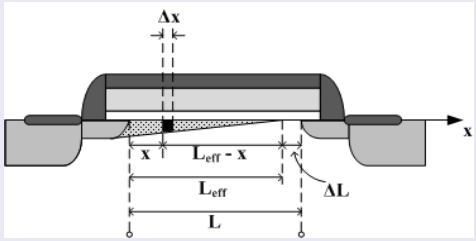

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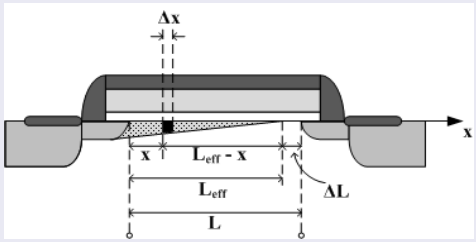

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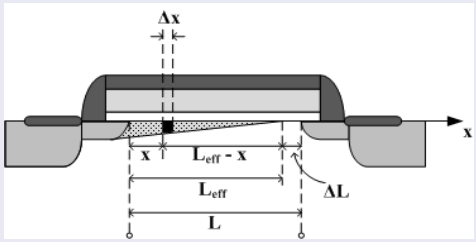

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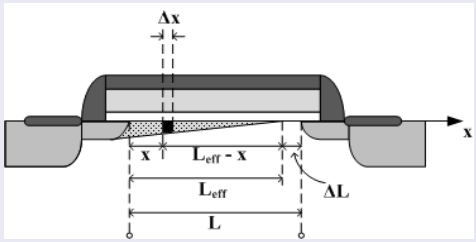

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- Incorporating SCE in PSD of drain noise current (Roy and Enz, TED 2005)
  - S.I. assumption (SCE dominant)
  - Two transistor approach
  - Effective mobility μ_{eff} varies w. E_x
- Thermal noise conductance
  - $G_{nD} = M \frac{W}{L_{eff}^2} \int_0^{L_{eff}} \mu_z \frac{T_C}{T_L} (-Qi(x)) dx$
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  - G_{nD} and G_{ds0} calculated at different operating points
  - Less relevant for circuit design

- Thermal noise excess factor: $\gamma = \frac{G_{nD}}{G_m}$
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  - Characterizes noise performance of transconductors
  - Used in noise calculation of cascode LNA: $F_{min} = 1 + 2\gamma\frac{\omega}{\omega_T}\sqrt{\frac{\beta_G}{\gamma}(1-c)^2}$
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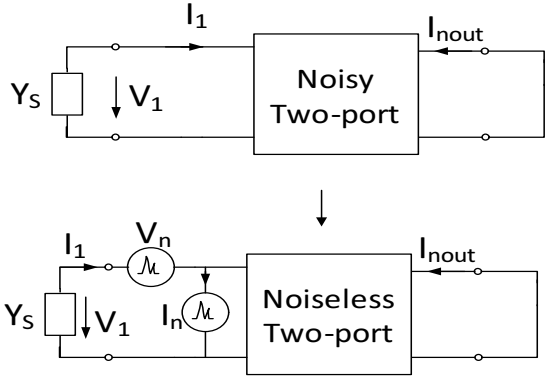
- Noise generated by any two-port device
  - Noiseless network w. two partially correlated noise sources
  - 4 noise parameters



- $F = F_{min} + \frac{R_n}{G_s}|Y_s - Y_{opt}|^2$
  - Minimum noise figure, F_{min}
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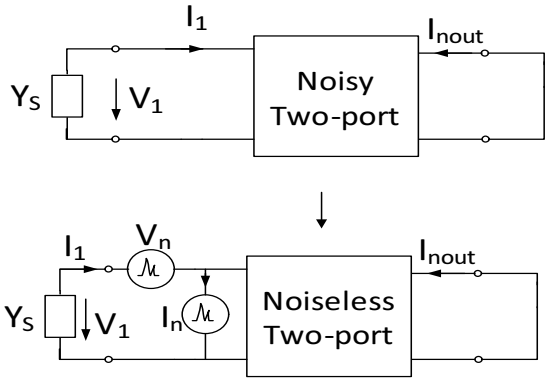

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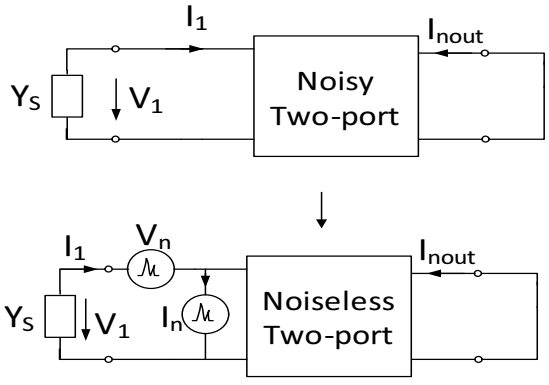

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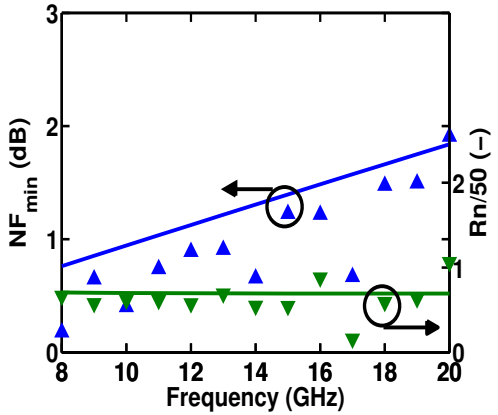
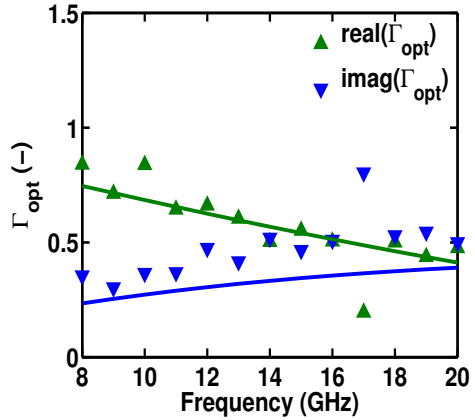
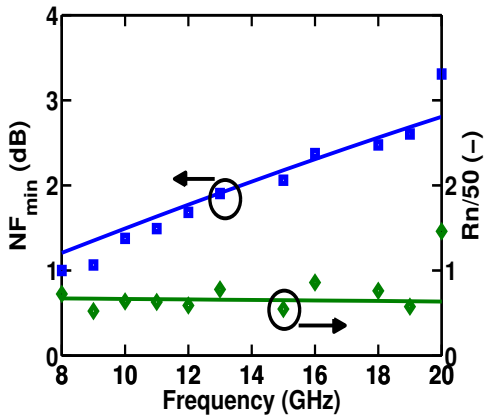
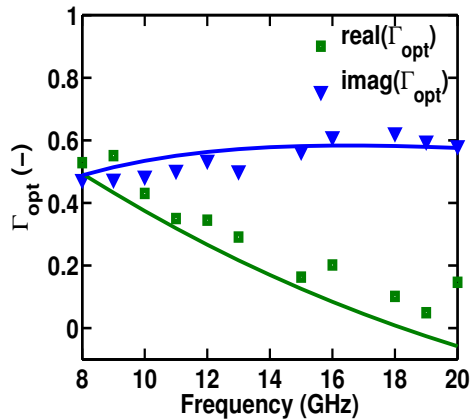




- NMOS ($L = 240nm$, $W = 40x2um$, $V_{GS} = 0.65V$, $V_{DS} = 1.2V$)





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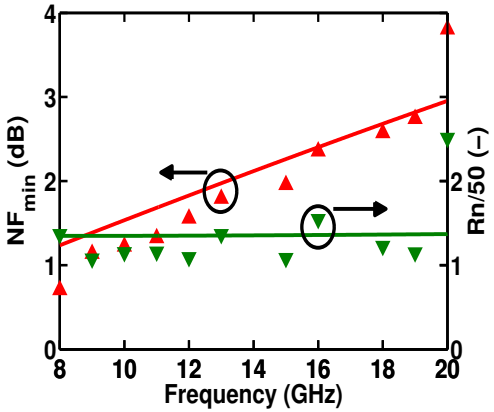

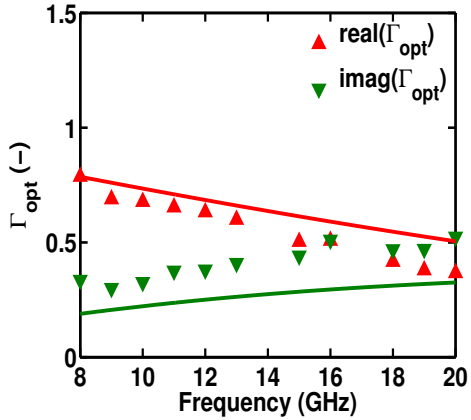

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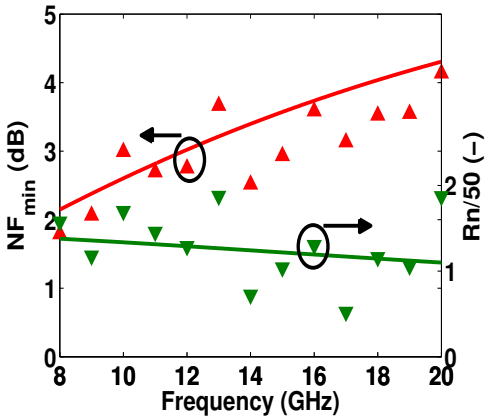
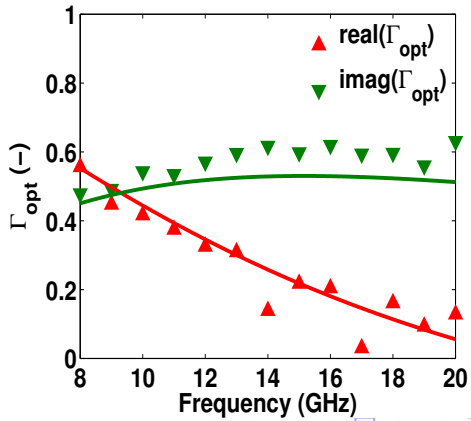
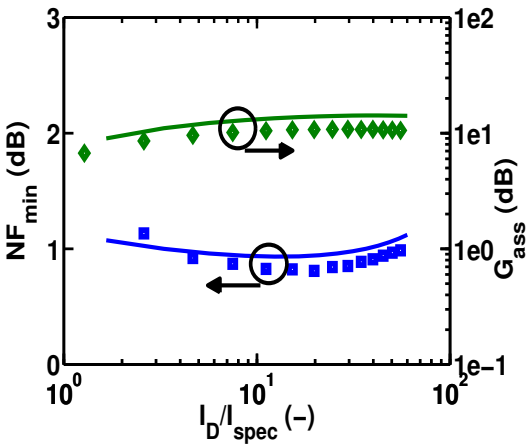
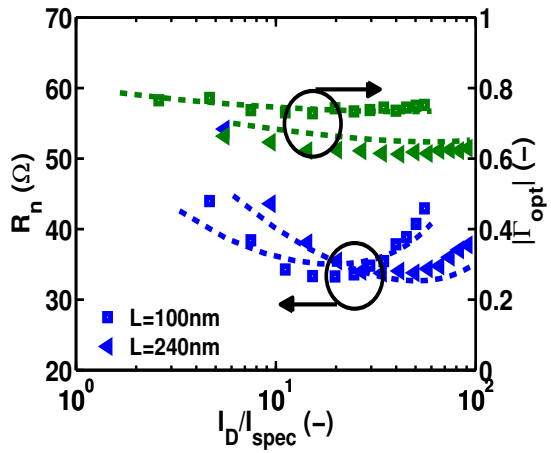


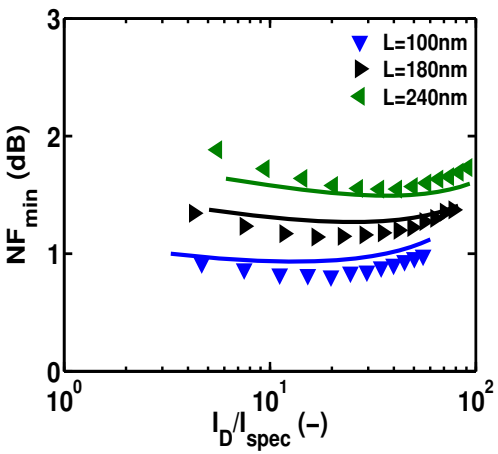


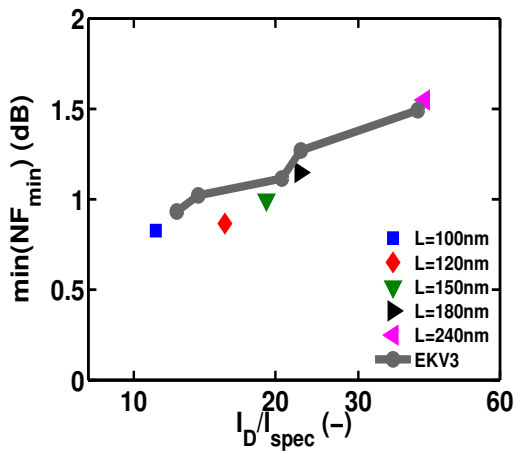
HF Noise Parameters vs. Bias

- NMOS ($W = 40x2um$, $V_{DS} = 1.2V$, $f = 10GHz$)





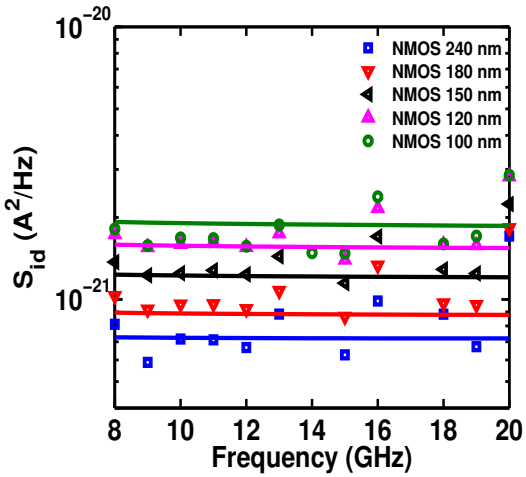


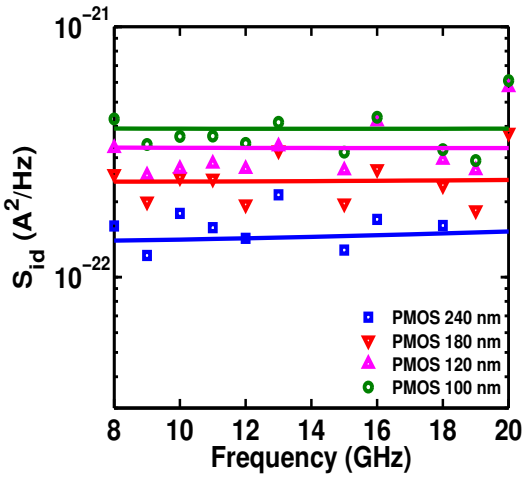


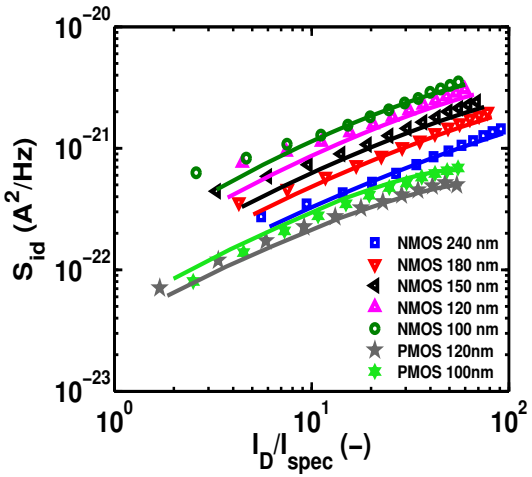
Antonopoulos et al., RFIC Symp. 2013

PSD of Drain Noise Current

- NMOS and PMOS($W = 40x2um, |V_{DS}| = 1.2V$)







Antonopoulos et al., IJNM 2014

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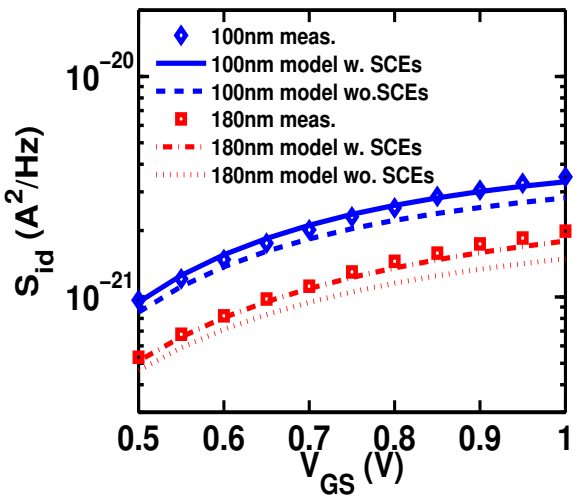

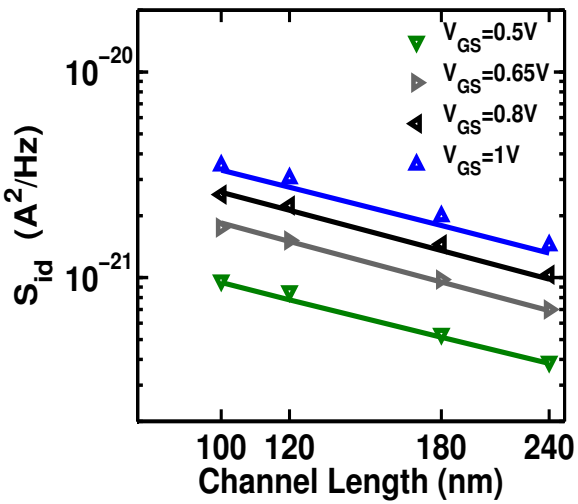

Antonopoulos et al., TED 2013

Design Parameters

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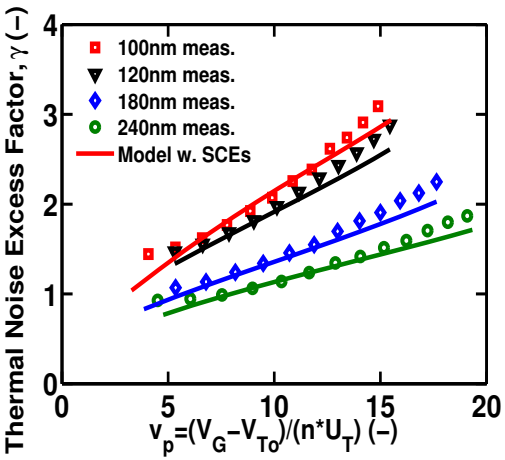
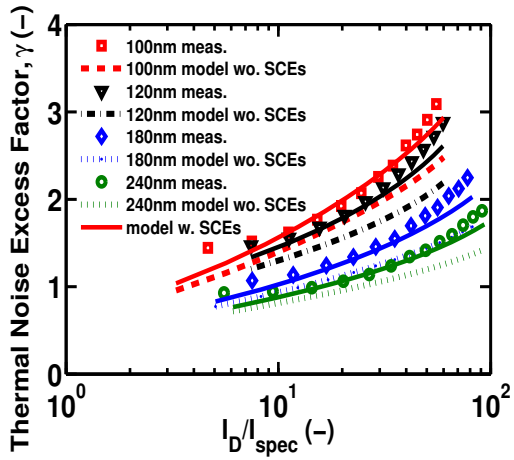
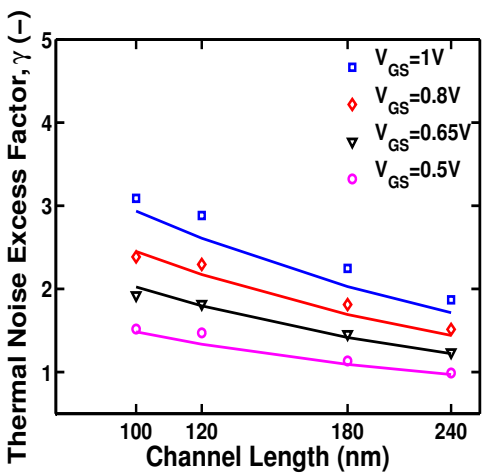
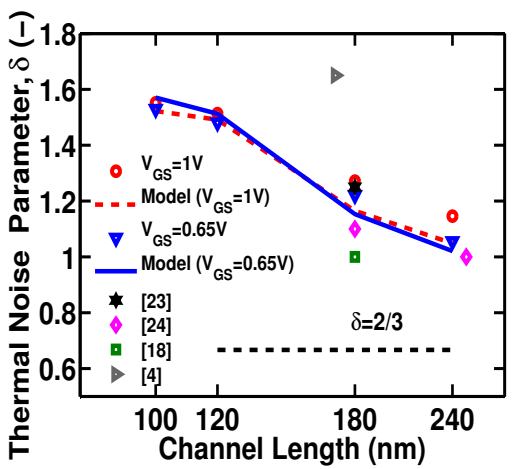


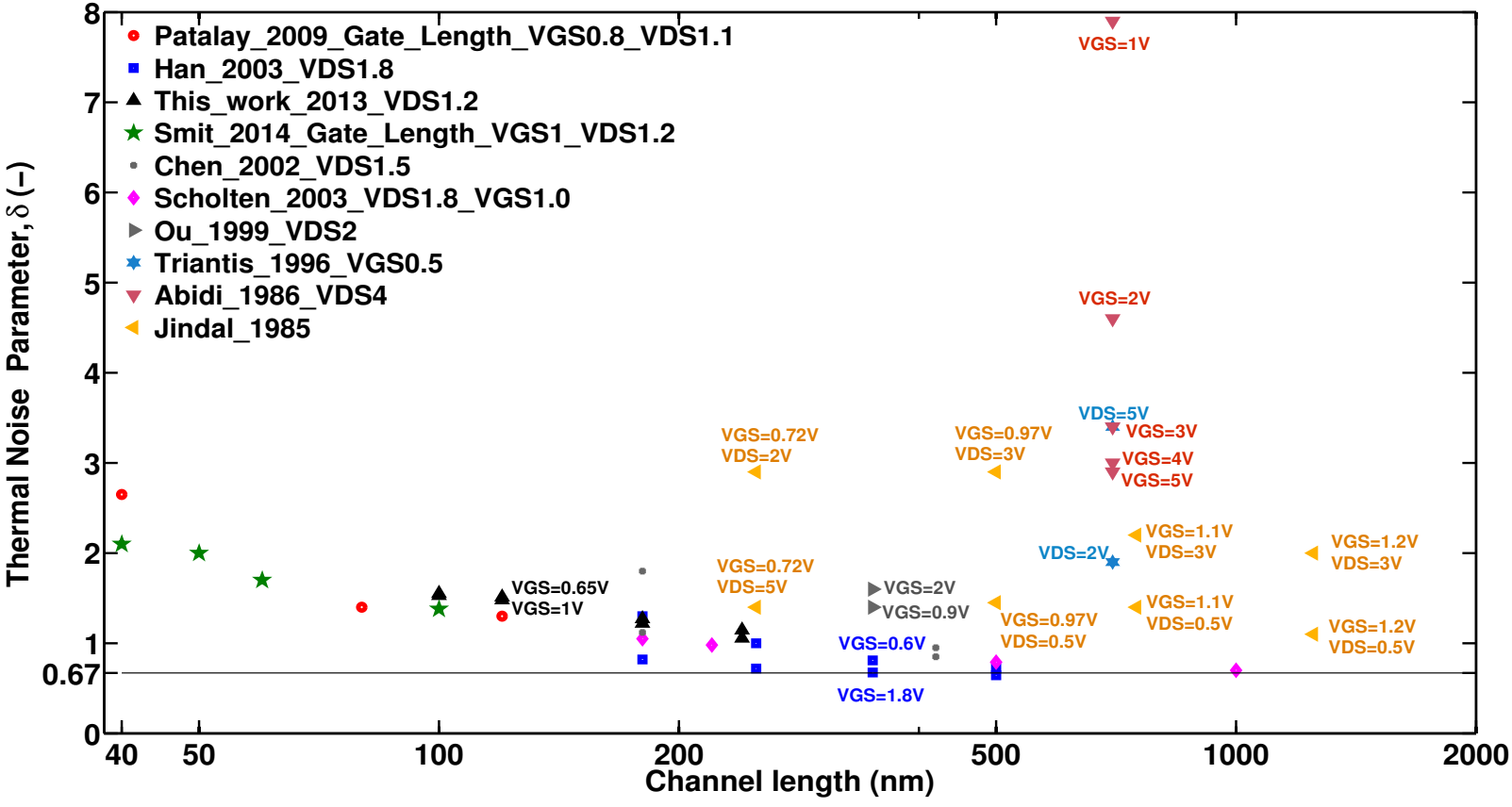






Antonopoulos et al., TED 2013

Thermal Noise Parameter, δ



Gate Current Noise

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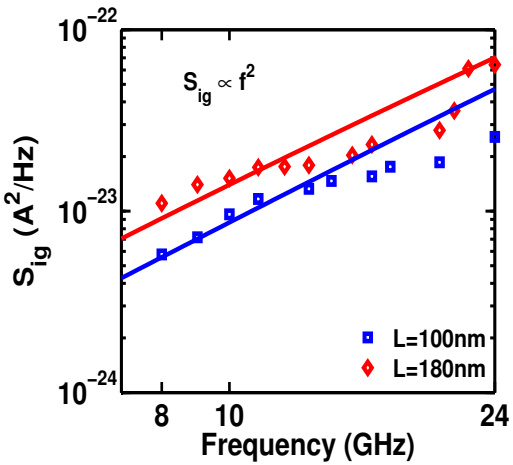

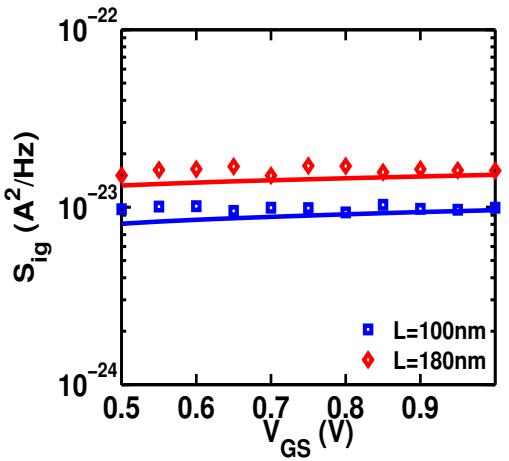

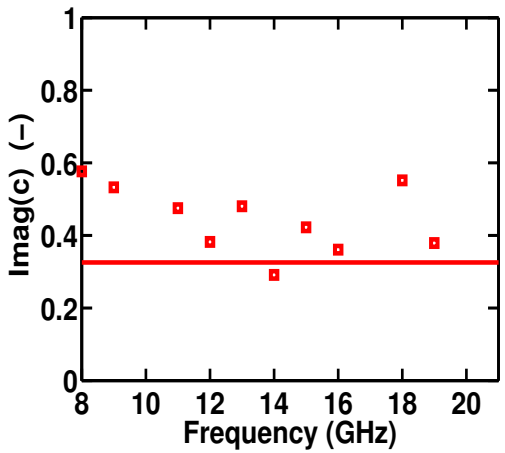

Antonopoulos et al., TED 2013

Conclusions on High Frequency Noise

- Detailed investigation of RF noise in MOSFETs in the context of circuit design
  - Frequency, L, and bias
- Thermal noise excess factor measurements for the first time
- SCE on thermal noise and γ
  - VS, CH, CLM
- Optimum noise performance
  - Vicinity of S.I. to M.I.

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- Thermal noise excess factor measurement and modeling for the first time
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- SNIM technique
  - Use minimum L to achieve high f_T
  - Calculate C_{gs} and W from $Z_{opt} = Real(Z_S)$
    - $G_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)}$
  - Calculate L_S from a given power constraint from $Real(Z_{in}) = Real(Z_S)$
    - $Real(Z_{in}) = \frac{g_m L_S}{C_{gs}}$
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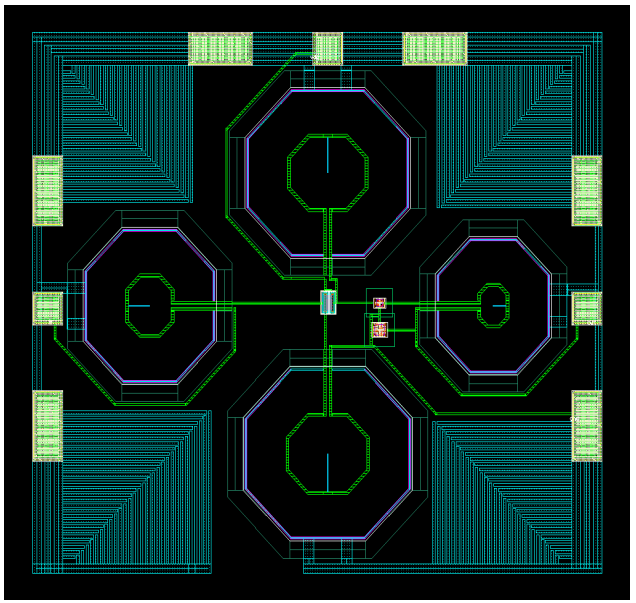
- Uppermost metal (M9) for interconnect lines
- Same orientation for all components
- Interaction between transmission lines and inductors should be avoided
- Width of interconnect lines determined by the current they have to drive
- Pad's capacitance as low as possible
- 0.3762 mm^2



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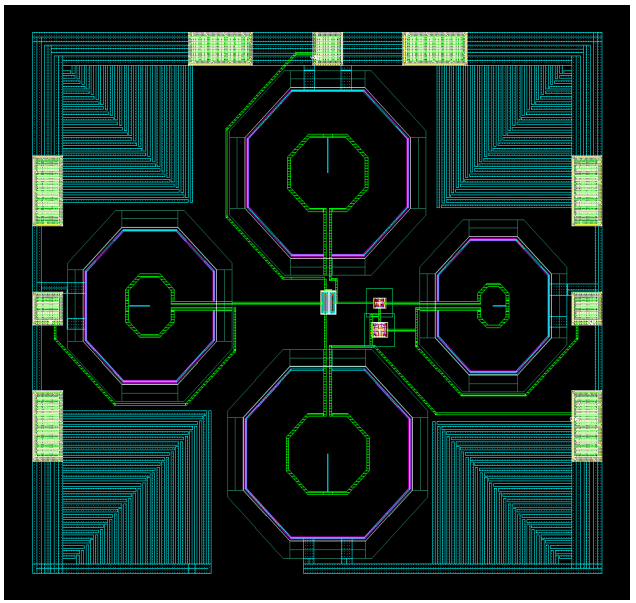

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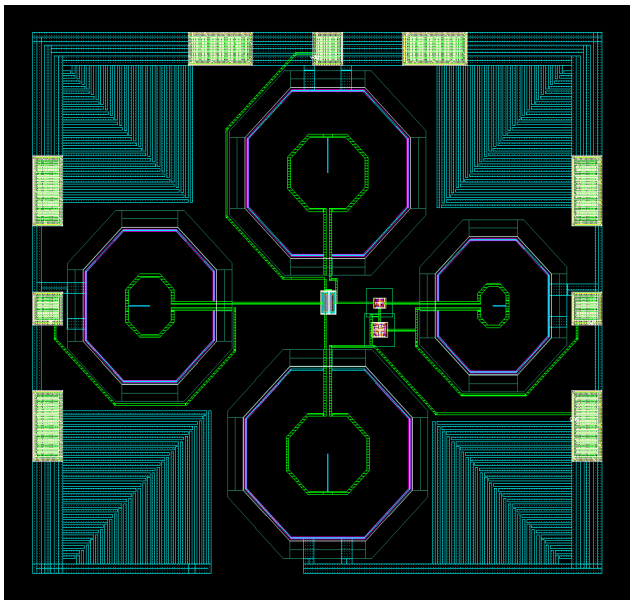

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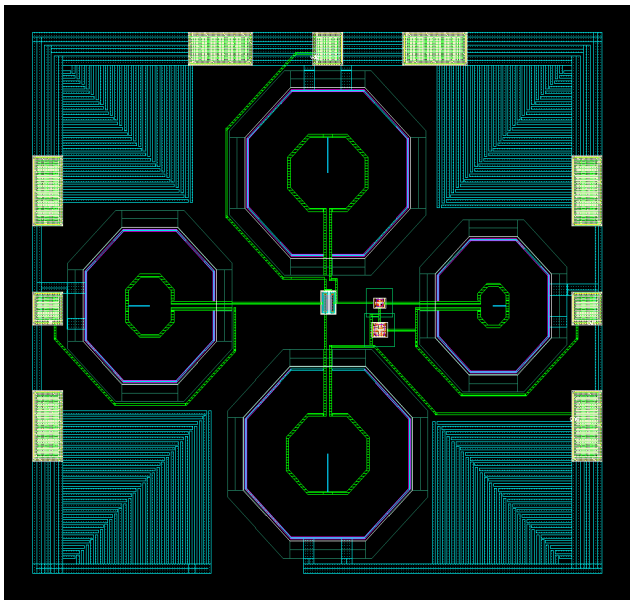

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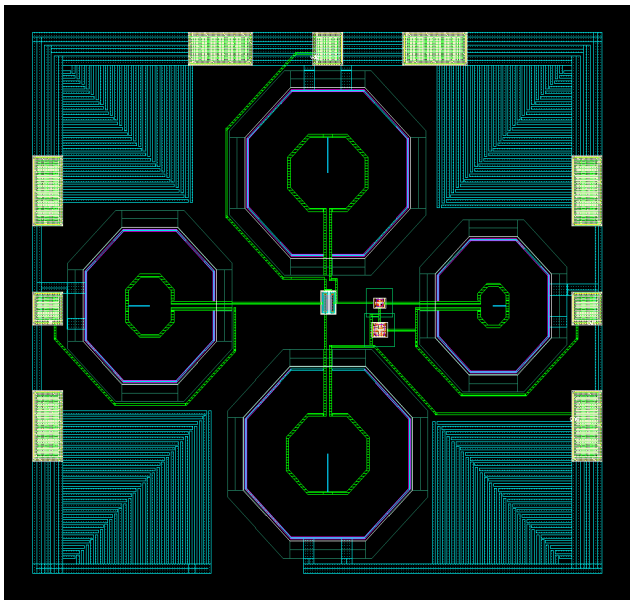

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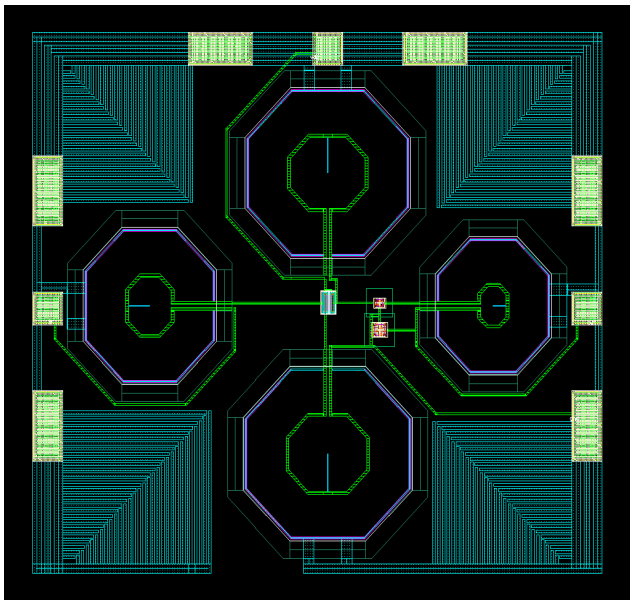
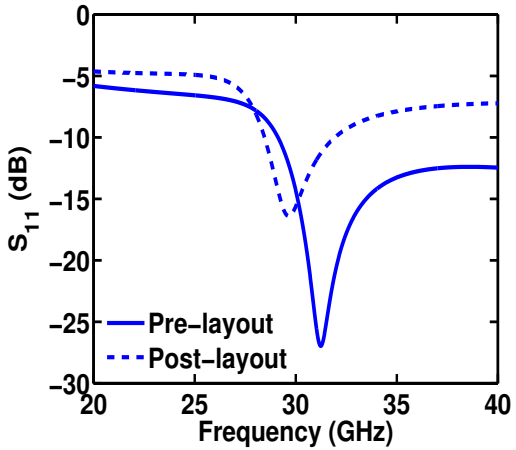
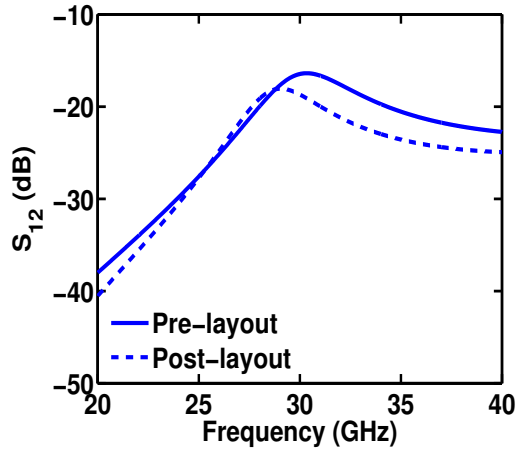
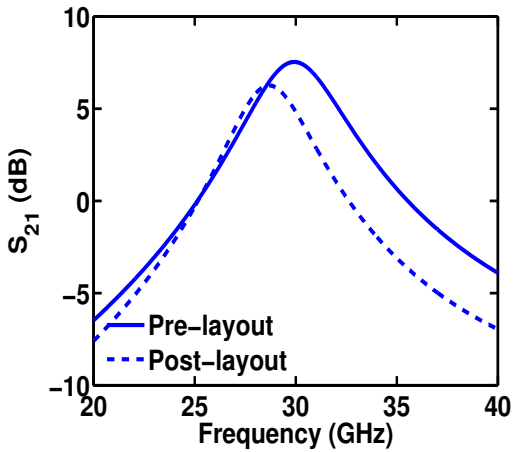
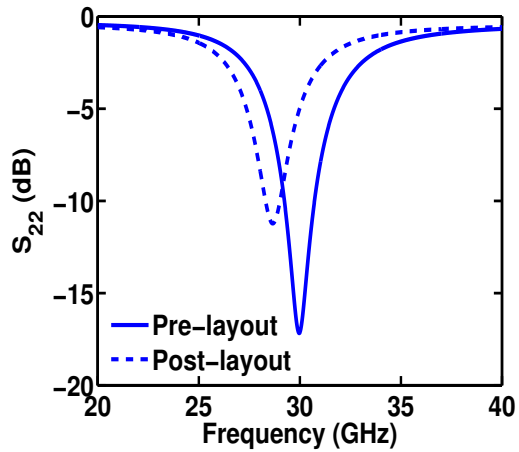


30 GHz LNA S-Parameters

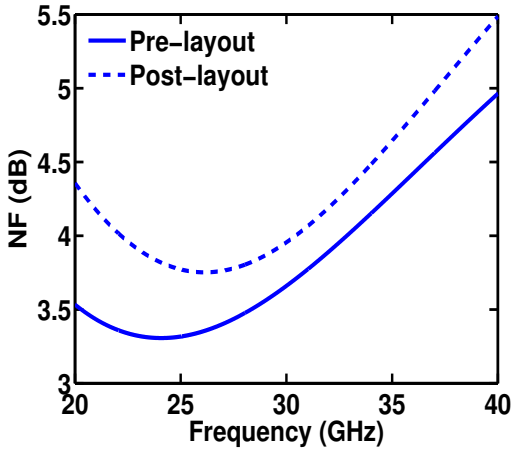


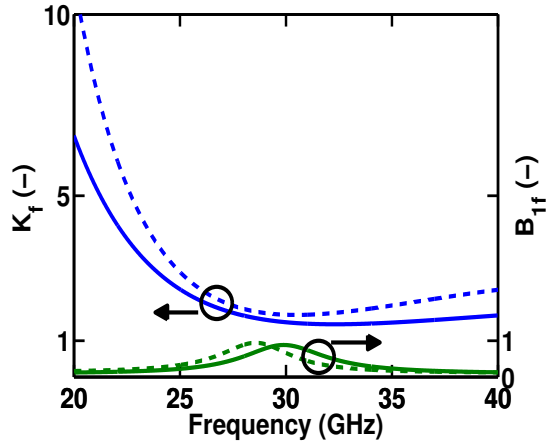


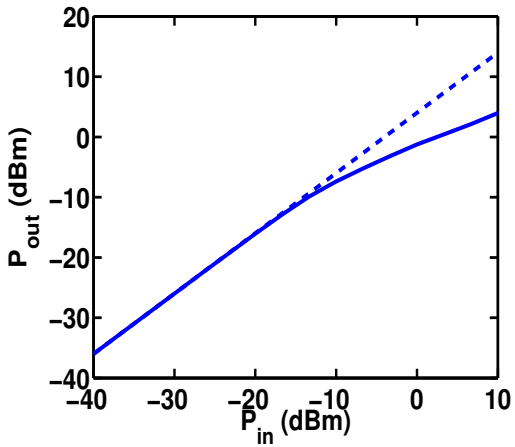


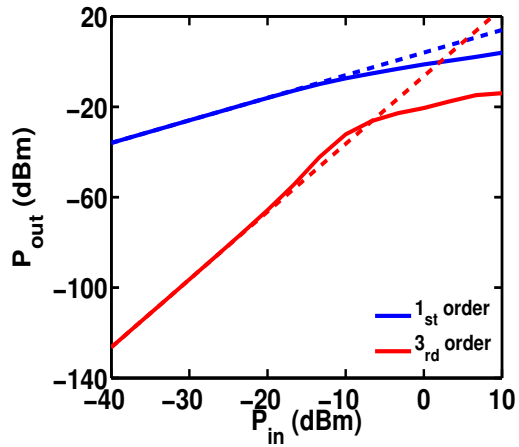


30 GHz LNA Noise, Stability, Linearity









30 GHz Single-Stage LNA Overall FoM

- $FoM = \frac{Gain(dB) \cdot IIP3(mW) \cdot f_c(GHz)}{(NF-1)(abs) \cdot P_{DC}(mW)}$

	This work ICCDCS 2012	Abadi et al. RFIC 2007	Yu et al. MWCL 2004	Ribeiro et al. EUROCON 2011	Sanduleanu et al. RFIC 2006
Process (nm)	**90**	90	180	130	90
Freq. (GHz)	**28.9**	28.5	25.7	30	32.5
S_{21} (dB)	**5.9**	20	8.9	7.4	18.6
NF (dB)	**3.9**	2.9	6.9	3.7	3
IIP3 (dB)	**4.9**	-7.5	2.8	6	-
P_{DC} (mW)	**7.2**	16.2	54	7	10
Area (mm^2)	**0.37**	0.67	0.73	0.17*	0.85
FoM (-)	**25.3**	3.3	1.4	45.8	-

5 GHz WiMAX LNA Design

- System level analysis of WiMAX RX
  - $NF = 3dB$, $Gain = 18dB$ (could be relaxed)
- Operation at $5.3GHz$
- Based on cascode topology (Andreani et al., CAS2 2001)
- **Extracted EKV3** model rather than the commercial one
- Bias in **M.I.** region via $(G_m/I_D) \cdot f_T$
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  - $I_D = 1.47mA$
  - IC close to the center of M.I.

5 GHz WiMAX LNA Design

- System level analysis of WiMAX RX
  - $NF = 3dB$, $Gain = 18dB$ (could be relaxed)
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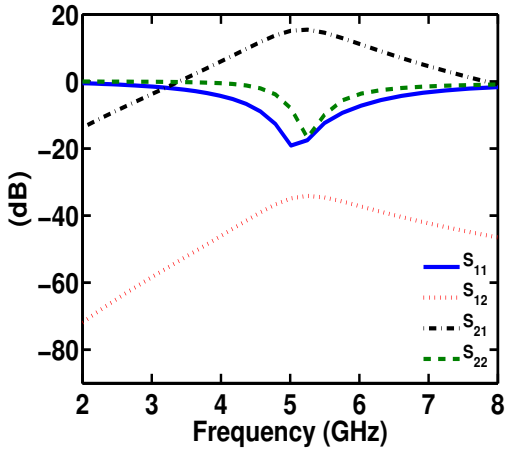
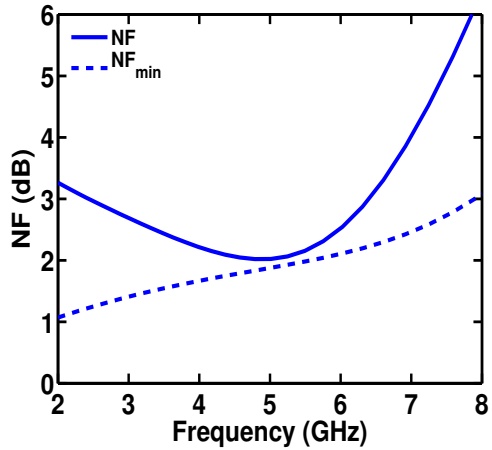
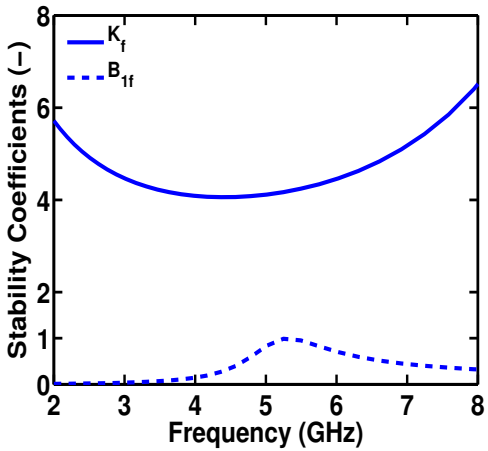
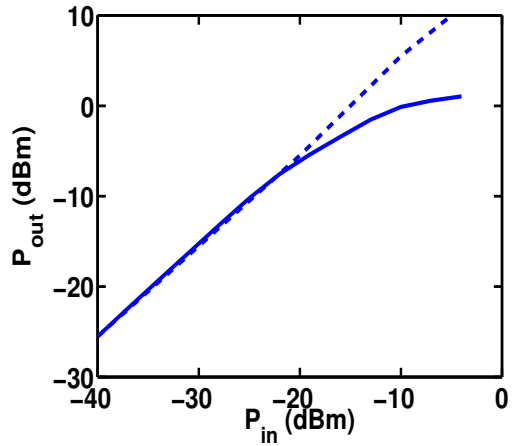
5 GHz WiMAX LNA Results



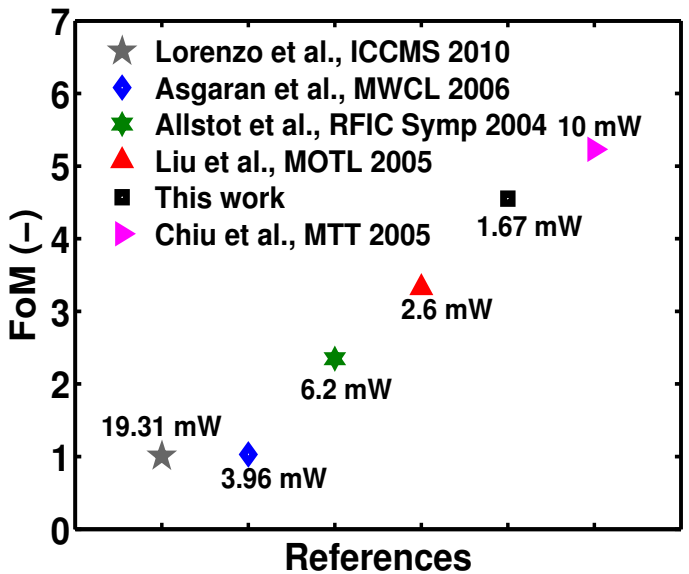






5 GHz WiMAX LNA Overall FoM

- High overall performance ($FoM = \frac{Gain(dB)\cdot IIP3(mW)\cdot f_c(GHz)}{(NF-1)(abs)\cdot P_{DC}(mW)}$)



Conclusions on LNA Design

- Device to circuit via $(G_m/I_D) \cdot f_T$ FoM
- Fairly high overall performance
- Low power consumption
- M.I. ideal for LNA design

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Final Conclusions

- Low-power RF CMOS transceiver design
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  - Design, layout and fabrication of an RF Test Chip w. a 30 GHz LNA
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  - Importance in terms of RFIC design highlighted
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  - Impact of SCE
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Journal Publications

1. **A. Antonopoulos**, M. Bucher, K. Papathanasiou, N. Mavredakis, N. Makris, R. K. Sharma, P. Sakalas, M. Schroter, "CMOS Small-Signal and Thermal Noise Modeling at High Frequencies", *IEEE Trans. Electron Devices*, Vol. 60, No. 11, November 2013.

2. **A. Antonopoulos**, M. Bucher, K. Papathanasiou, N. Makris, N. Mavredakis, R. K. Sharma, P. Sakalas, M. Schroter, "Modeling of High Frequency Noise of Silicon MOS Transistors for RFIC Design", *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, special issue on Modeling of high-frequency silicon transistors*, in press.

3. W. Grabinski, M. Brinson, P. Nenzi, F. Lannutti, N. Makris, **A. Antonopoulos**, M. Bucher, "Open source circuit simulation tools for RF compact semiconductor device modelling", *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, special issue on Modeling of high-frequency silicon transistors*, invited paper, in press.

Conference Publications

1. **A. Antonopoulos**, M. Bucher, K. Papathanasiou, N. Makris, R. K. Sharma, P. Sakalas, M. Schroter, "CMOS RF Noise, Scaling, and Compact Modeling for RFIC Design", *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 53-56, Seattle, June 2013.
2. R.K Sharma, **A. Antonopoulos**, N. Mavredakis, M. Bucher, "Impact of Design Engineering on RF Linearity and Noise Performance of Nanoscale DG SOI MOSFETs", *14th International Conference on Ultime Integration on Silicon (ULIS),* pp. 145-148, Coventry, 2013.
3. **A. Antonopoulos**, K. Papathanasiou, M. Bucher, K. Papathanasiou, "CMOS LNA Design at 30 GHz – A Case Study", *8th International Caribbean Conference on Devices Circuits and Systems (ICCDCS)*, pp. 1-4, Playa Del Carmen, 2012.
4. R. K. Sharma, **A. Antonopoulos**, N. Mavredakis, M. Bucher, "Analog/RF Figures of Merit of Advanced DG MOSFETs", *8th International Caribbean Conference on Devices Circuits and Systems (ICCDCS)*, pp. 1-4, Playa Del Carmen, 2012.
5. K. Papathanasiou, N. Makris, **A. Antonopoulos**, M. Bucher, "Moderate inversion: analog and RF benchmarking of the EKV3 compact model", *29th International Conference on Microelectronics (MIEL)*, Belgrade, May 12-14, 2014, accepted.

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Ευρωπαϊκή Ένωση
Ευρωπαϊκό Κοινωνικό Ταμείο

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Με τη συγχρηματοδότηση της Ελλάδας και της Ευρωπαϊκής Ένωσης

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